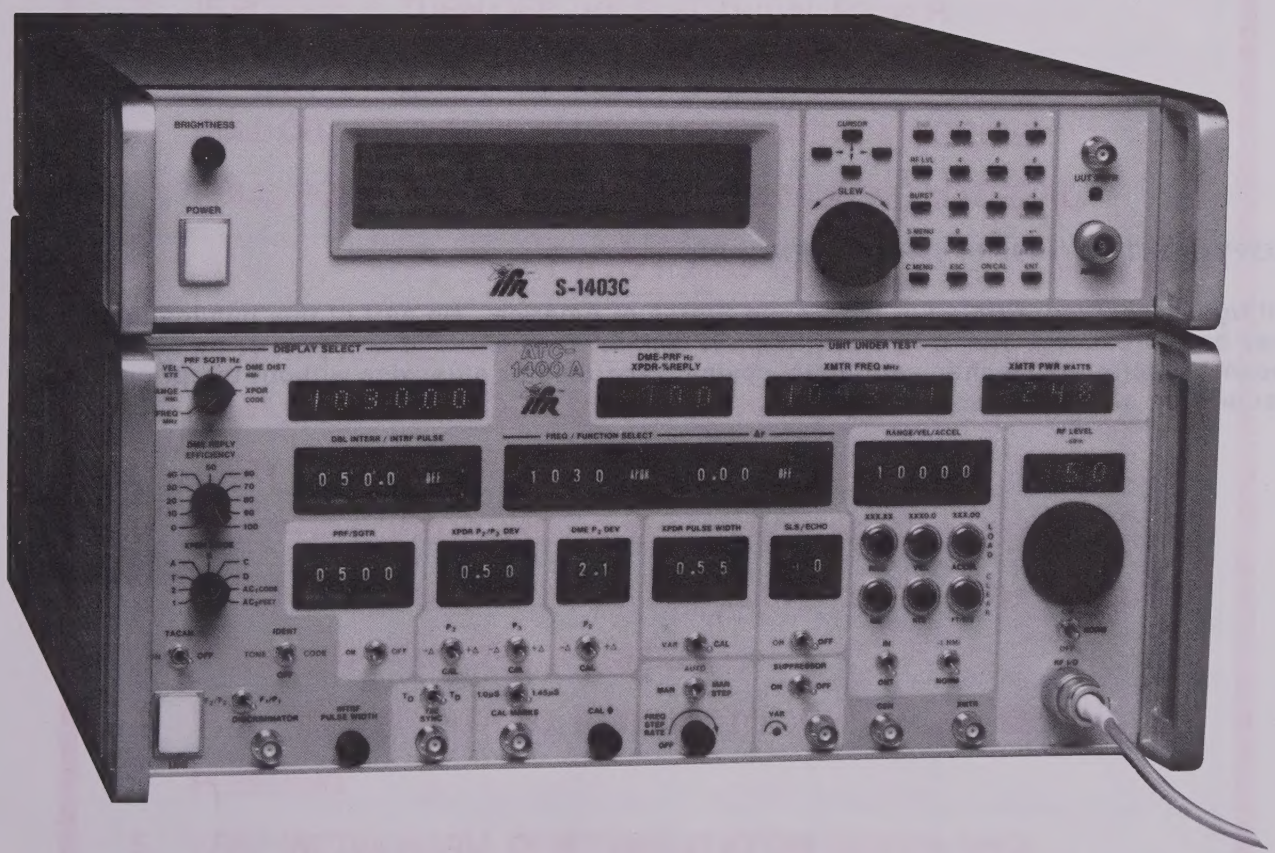
# MAINTENANCE MANUAL

# MODE S
## TEST SYSTEM

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MAINTENANCE MANUAL
MODE S TEST SYSTEM

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# WARNING

## HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

## RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM.
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, ROPE OR SOME OTHER DRY INSULATING MATERIAL.

## FIRST AID

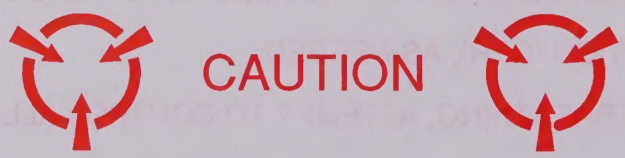
1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. CALL FOR DOCTOR AND/OR AMBULANCE, IMMEDIATELY.
3. IF BREATHING HAS STOPPED; ADMINISTER CARDIO-PULMONARY RESUSCITATION (CPR), AS NEEDED.
4. IF VICTIM IS BREATHING, ATTEMPT TO CONTROL ALL SERIOUS BLEEDING.
5. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.

**CAUTION:** INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FETS, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

- BEFORE USE IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.
- WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.
- TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.
- DEVICES MUST NEVER BE INSERTED INTO NOR REMOVED FROM CIRCUITS WITH POWER ON.
- PC BOARDS, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG. REMOVE ANY BUILT-IN POWER SOURCE, SUCH AS A BATTERY, BEFORE LAYING PC BOARDS ON A CONDUCTIVE MAT OR STORING IN A CONDUCTIVE CONTAINER.
- PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BAG.

**CAUTION:** THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO AVIATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO AERONAUTICAL SERVICE OUT TO A DISTANCE OF SEVERAL MILES.

**CAUTION:** USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND ENSURE COMPLIANCE WITH INSTRUCTIONS IN FAA CIRCULAR AC 170-6C, DATED FEBRUARY 19, 1981.



## RECORD OF REVISIONS

| REV NO. | ISSUE DATE | DATE INSERTED | BY | REV NO. | ISSUE DATE | DATE INSERTED | BY |
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# LIST OF EFFECTIVE PAGES

| Chapter/Section/Subject | Page | Date |
|---|---|---|
| Title Page | | May 1/93 |
| Copyright Page | | May 1/93 |
| Warning Page | | May 1/93 |
| Caution Page | | May 1/93 |
| Record of Revisions | | May 1/93 |
| List of Effective Pages | 1 through 2 | May 1/93 |
| Table of Contents | 1 through 2 | May 1/93 |
| Introduction | 1 through 2 | May 1/93 |
| 2-Table of Contents | 1 through 2 | May 1/93 |
| 2-List of Illustrations | 1 through 2 | May 1/93 |
| 2-List of Tables | 1 through 2 | May 1/93 |
| 2-1-1 | 1 through 4 | May 1/93 |
| 2-2-1 | 1 through 46 | May 1/93 |
| 2-2-2 | 1 through 32 | May 1/93 |
| 2-2-3 | 1 through 28 | May 1/93 |
| 2-3-1 | 1 through 30 | May 1/93 |
| 2-3-2 | 1 through 2 | May 1/93 |
| Appendix A | 1 through 4 | May 1/93 |
| Appendix B | 1 through 4 | May 1/93 |
| Appendix C | 1 through 2 | May 1/93 |
| Appendix D | 1 through 2 | May 1/93 |
| Index | 1 through 8 | May 1/93 |

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# TABLE OF CONTENTS


| Title | Chapter/Section |
|---|---|
| Title Page | |
| Copyright Page | |
| Warning Page | |
| Caution Page | |
| Record of Revisions | |
| List of Effective Pages | |
| Table of Contents | |
| Introduction | |
| Chapter 2 | |
| Servicing | 2-1 |
| Troubleshooting | 2-2 |
| Disassembly/Reassembly | 2-3 |
| Appendix A - Connector Pin-Out Tables | |
| Appendix B - Abbreviations | |
| Appendix C - Test Equipment Requirements | |
| Appendix D - Metric/British Imperial Conversion Table with Nautical Distance Conversions | |
| Index | |

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# INTRODUCTION - MODE S TEST SYSTEM

This manual contains the information necessary to test and repair the Mode S Test System consisting of the S-1403C Test Auxiliary (with or without the Multi-Level Diversity [MLD] option installed) and the ATC-1400A Transponder/DME Test Set. The Mode S Test System Maintenance Manual is designed for use with the ATC-1400A Maintenance Manual.

It is strongly recommended that personnel be thoroughly familiar with the contents of this manual before attempting to perform maintenance on this equipment.

## ORGANIZATION

This manual is divided into three sections as follows:

CHAPTER 2 - MAINTENANCE

Section 1 - SERVICING (preventive maintenance)

Section 2 - TROUBLESHOOTING (theory of operation; calibration\verification; PC boards and schematics)

Section 3 - DISASSEMBLY/REASSEMBLY (disassembly; reassembly)

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# CHAPTER TWO

# MODE S TEST SYSTEM

# MAINTENANCE MANUAL

# TABLE OF CONTENTS


| Title | Chapter/Section/Subject | Page |
|---|---|---|
| SECTION 1 - SERVICING | 2-1 | |
| 1. Preventive Maintenance Procedures | 2-1-1 | 1 |
| A. External Cleaning | 2-1-1 | 1 |
| B. Internal Cleaning | 2-1-1 | 1 |
| C. Visual Inspection | 2-1-1 | 2 |
| SECTION 2 - TROUBLESHOOTING | 2-2 | |
| 1. Theory of Operation | 2-2-1 | 1 |
| A. General | 2-2-1 | 1 |
| B. System Overview | 2-2-1 | 1 |
| (1) Mode S Function | 2-2-1 | 1 |
| (2) Major Operating Characteristics | 2-2-1 | 1 |
| (3) Basic System Protocol | 2-2-1 | 2 |
| (4) Mode S Message Content | 2-2-1 | 2 |
| C. System Theory of Operation | 2-2-1 | 2 |
| (1) General | 2-2-1 | 2 |
| (2) S-1403C to ATC-1400A Communications | 2-2-1 | 3 |
| D. Functional Theory of Operation | 2-2-1 | 4 |
| (1) Introduction | 2-2-1 | 4 |
| (2) Receive | 2-2-1 | 5 |
| (3) Transmit | 2-2-1 | 6 |
| (4) Test Validity | 2-2-1 | 7 |
| D. Module Theory of Operation | 2-2-1 | 7 |
| (1) Power Supply | 2-2-1 | 7 |
| (2) Processor PC Board Assembly | 2-2-1 | 11 |
| (3) Front Panel Assembly | 2-2-1 | 18 |
| (4) Pulse PC Board Assembly | 2-2-1 | 24 |
| (5) Diversity Module | 2-2-1 | 34 |
| (6) Attenuator Assembly (Only with MLD) | 2-2-1 | 45 |
| 2. Calibration/Verification | 2-2-2 | 1 |
| A. General | 2-2-2 | 1 |
| (1) Calibration/Verification Schedule | 2-2-2 | 1 |
| (2) Controls, Connectors and Indicators | 2-2-2 | 1 |
| (3) Disassembly Requirements | 2-2-2 | 1 |
| B. Performance Requirements | 2-2-2 | 1 |
| C. Test Equipment Requirements | 2-2-2 | 2 |
| D. Preliminary Operations | 2-2-2 | 2 |
| (1) Safety Precautions | 2-2-2 | 2 |
| (2) Environmental Considerations | 2-2-2 | 2 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| E. Test Record | 2-2-2 | 2 |
| F. Calibration/Verification Procedures | 2-2-2 | 5 |
| (1) Power Supply | 2-2-2 | 5 |
| (2) Interrogation Pulses and SPR | 2-2-2 | 7 |
| (3) Suppressor and Interference Pulses | 2-2-2 | 13 |
| (4) RF Level | 2-2-2 | 16 |
| (5) Antenna B | 2-2-2 | 18 |
| (6) Reply Delay and PPMG | 2-2-2 | 22 |
| G. Calibration/Verification Data Sheet | 2-2-2 | 26 |
| 3. PC Boards and Schematics | 2-2-3 | 1 |
| A. General | 2-2-3 | 1 |
| B. How To Use Schematics | 2-2-3 | 1 |
| (1) Coaxial Cables | 2-2-3 | 1 |
| (2) Multiple Pin Connectors | 2-2-3 | 1 |
| C. Alphabetical Index of Assemblies, Interconnect Diagrams and Circuit Schematics | 2-2-3 | 2 |
| SECTION 3 - DISASSEMBLY/REASSEMBLY | 2-3 | |
| 1. Disassembly | 2-3-1 | 1 |
| A. General | 2-3-1 | 1 |
| B. Preliminary Considerations | 2-3-1 | 1 |
| (1) Tools Required | 2-3-1 | 1 |
| (2) Disassembly Precautions | 2-3-1 | 1 |
| C. Disassembly Procedures | 2-3-1 | 5 |
| (1) Chassis Assembly | 2-3-1 | 5 |
| (2) Power Supply Assembly | 2-3-1 | 5 |
| (3) Line Supply Assembly | 2-3-1 | 9 |
| (4) Processor and Pulse PC Board Assemblies | 2-3-1 | 10 |
| (5) Front Panel Assembly | 2-3-1 | 11 |
| (6) Diversity Module | 2-3-1 | 14 |
| (7) Motherboard PC Board Assembly | 2-3-1 | 27 |
| (8) Attenuator Assembly (w/ MLD) | 2-3-1 | 28 |
| 2. Reassembly | 2-3-2 | 1 |
| A. General | 2-3-2 | 1 |
| B. Preliminary Considerations | 2-3-2 | 1 |
| (1) Tools Required | 2-3-2 | 1 |
| (2) Reassembly Precautions | 2-3-2 | 1 |
| C. Reassembly Procedures | 2-3-2 | 2 |
| (1) General | 2-3-2 | 2 |
| (2) Power Termination Assembly | 2-3-2 | 2 |

# LIST OF ILLUSTRATIONS


| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Mode S System Block Diagram | 2-2-1 | 3 |
| System Receive Block Diagram | 2-2-1 | 5 |
| System Transmit Block Diagram | | 6 |
| Line Supply PC Board Assembly Block Diagram | 2-2-1 | 7 |
| Inverter Supply PC Board Assembly Block Diagram | 2-2-1 | 9 |
| Processor PC Board Asembly Block Diagram | 2-2-1 | 11 |
| Processor/System Memory Block Diagram | 2-2-1 | 12 |
| Processor PC Board Communications Block Diagram | 2-2-1 | 15 |
| Front Panel Assembly Block Diagram | 2-2-1 | 18 |
| Slew Control Timing Diagram | 2-2-1 | 20 |
| Pulse PC Board Assembly Block Diagram | 2-2-1 | 25 |
| Pulse Generator Data Transfer Timing Chart | 2-2-1 | 27 |
| Edge Detect Block Diagram | 2-2-1 | 29 |
| Diversity Module w/o MLD Block Diagram | 2-2-1 | 35 |
| Diversity Module w/ MLD Block Diagram | 2-2-1 | 35 |
| 1030 MHz Source PC Board Assembly Block Diagram | 2-2-1 | 36 |
| Power Amp PC Board Assembly Block Diagram | 2-2-1 | 38 |
| Modulator Assembly w/o MLD Block Diagram | 2-2-1 | 39 |
| Modulator Assembly w/ MLD Block Diagram | 2-2-1 | 40 |
| Attenuator Assembly Block Diagram | 2-2-1 | 45 |
| S-1403C Front and Rear Panels | 2-2-2 | 3 |
| ATC-1400A Front and Rear Panels | 2-2-2 | 4 |
| Test Points and Adjustments | 2-2-2 | 6 |
| Interrogation Pulses and SPR Test Setup Diagram | 2-2-2 | 7 |
| $P_6$ Amplitude Example | 2-2-2 | 10 |
| $P_2$ to SPR Spacing/Phase Transition Time | 2-2-2 | 11 |
| Suppressor and Interference Pulses Test Setup Diagram | 2-2-2 | 13 |
| Antenna B Test Setup Diagram | 2-2-2 | 18 |
| Reply Delay and PPG Test Setup Diagram | 2-2-2 | 22 |
| Pulse PC Board Assembly Jumper Terminal Blocks | 2-2-2 | 25 |
| Composite Assembly | 2-2-3 | 3 |
| Line Supply PC Board Assembly | 2-2-3 | 5 |
| Power Supply Assembly | 2-2-3 | 6 |
| Processor PC Board Assembly | 2-2-3 | 8 |
| Front Panel Assembly | 2-2-3 | 11 |
| Pulse PC Board Assembly | 2-2-3 | 16 |
| Motherboard PC Board Assembly | 2-2-3 | 18 |
| Diversity Module | 2-2-3 | 19 |
| Attenuator Assembly | 2-2-3 | 28 |
| S-1403C Composite Disassembly (w/o MLD) | 2-3-1 | 3 |
| S-1403C Composite Disassembly (w/ MLD) | 2-3-1 | 4 |
| Line Supply PC Board Assembly Disassembly | 2-3-1 | 7 |
| Power Supply Assembly Disassembly | 2-3-1 | 8 |
| Front Panel Assembly Disassembly | 2-3-1 | 13 |
| Diversity Module (w/o MLD) | 2-3-1 | 15 |
| Diversity Module (w/ MLD) | 2-3-1 | 16 |
| Modulator Assembly Disassembly | 2-3-1 | 19 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Power Termination Assemlby Disassembly | 2-3-1 | 23 |
| Source/Pwr Amp Assembly Disassembly | 2-3-1 | 25 |
| Attenuator Assembly Disassembly | 2-3-1 | 29 |

# LIST OF TABLES


| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Microprocessor U12001 Chip Selects | 2-2-1 | 13 |
| LCD Control | 2-2-1 | 22 |
| Antenna B RF Vernier | 2-2-1 | 24 |
| Edge Detect Byte Formation | 2-2-1 | 31 |
| Disassembly Tools | 2-3-1 | 1 |

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# SECTION 1 - SERVICING

## 1. Preventive Maintenance Procedures

Contains routine maintenance instructions for cleaning and inspecting the Test Set.

**CAUTION:** DISCONNECT POWER FROM TEST SET TO AVOID POSSIBLE DAMAGE TO ELECTRONIC CIRCUITS.

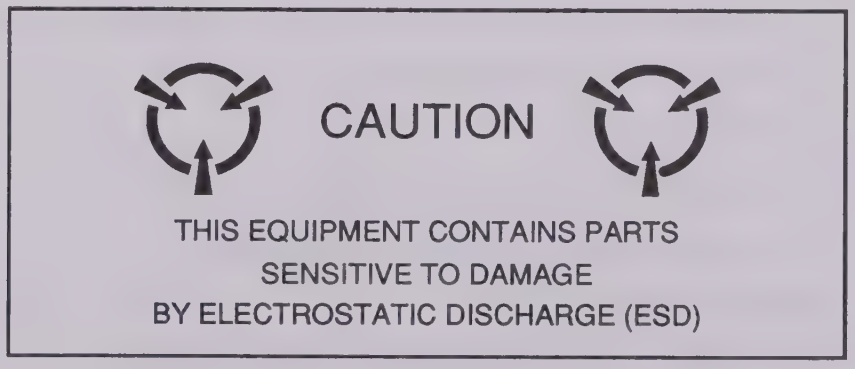
### A. External Cleaning

| STEP | PROCEDURE |
|---|---|

1. Clean front panel, switches and display face with soft lint-free cloth. If dirt is difficult to remove, dampen cloth with water and liquid detergent.
2. Remove fan filter from rear panel and remove dust with dry air jet. (If dirt is difficult to remove, wash filter in warm soapy water and dry with dry air jet.)
3. Remove grease, fungus and ground-in dirt from surfaces with soft lint-free cloth dampened (not wet) with denatured alcohol.
4. Remove dust and dirt from connectors with soft-bristled brush.

   **NOTE:** Cover connectors, not in use, with suitable dust cover to prevent tarnishing of connector contacts.
5. Clean cables with soft lint-free cloth.
6. Paint exposed metal surface to avoid corrosion.

### B. Internal Cleaning




**CAUTION:** DO NOT MOVE COMPONENTS ON CIRCUIT BOARDS OR DISASSEMBLE CONNECTORS NEEDLESSLY TO AVOID POSSIBLE DAMAGE.

**CAUTION:** DO NOT OPEN COMPLEX INTERNAL MODULES FOR SOLE PURPOSE OF CLEANING AND INSPECTION.

| STEP | PROCEDURE |
|---|---|

1. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm$^2$) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

2. Clean switches and controls with contact cleaner.

C. Visual Inspection

| STEP | PROCEDURE |
|---|---|

1. Inspect Chassis for:

   - Tightness of sub-assemblies and chassis mounted connectors.
   - Corrosion or damage to metal surfaces.

2. Inspect Capacitors for:

   - Loose mounting, deformities or obvious physical damage.
   - Leakage or corrosion around leads.

3. Inspect Connectors for loose or broken parts, cracked insulation and bad contacts.

4. Inspect Rotary Encoder for free rotation.

5. Inspect Circuit Boards for:

   - Corrosion or damage to connectors.
   - Damage to mounted components including crystals and ICs.
   - Freedom from foreign material.

6. Inspect Resistors for:

   - Cracked, broken, charred or blistered bodies.
   - Loose or corroded soldering connections.

7. Inspect Semiconductors for:

   - Cracked, broken, charred or discolored bodies.
   - Seals around leads being in place and in good condition.

8. Inspect Switches for:

   - Loose levers, terminals and switch body contact to frame.
   - Bent or loose line switch contacts.

STEP PROCEDURE

9. Inspect Wiring for:

   - Broken or loose ends and connections.
   - Proper dress relative to other chassis parts.

   **NOTE**: Verify laced wiring is tight with ends securely tied.

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# SECTION 2 - TROUBLESHOOTING

## 1. Theory of Operation

### A. General

Theory of Operation is divided into four levels as follows:

- System Overview

  Contains a description of the operation of Mode S in the ATC environment and a general overview of the principles associated with Mode S.

- System Theory of Operation

  Contains a simplified description of signal flow between the S-1403C and ATC-1400A. Refer to 2-2-1, Figure 1.

- Functional Theory of Operation

  Contains a simplified description of the functional groupings in the S-1403C, with accompanying block diagrams.

- Module Theory of Operation

  Contains a detailed description of each assembly or module in the S-1403C, with accompanying block diagrams.

### B. System Overview

#### (1) Mode S Function

Mode S is a cooperative surveillance and communication system for air traffic control using ground or air based interrogators and airborne transponders. Data link communications are accomplished integrally with surveillance interrogations (that may or may not be initiated by squitters) and replies. Mode S is an evolutionary addition to Air Traffic Control Radar Beacon System (ATCRBS), providing the enhanced surveillance and communication capability required for air traffic control automation. To facilitate the introduction of Mode S into the ATCRBS system, both ground and airborne Mode S installations include full ATCRBS capability. Mode S interrogators provide surveillance of ATCRBS-equipped aircraft and Mode S transponders are capable of replying to ATCRBS interrogations.

#### (2) Major Operating Characteristics

Mode S and ATCRBS use the same frequencies (1030 MHz for interrogations and 1090 MHz for replies). Mode S interrogations are transmitted using binary differential phase shift keying (DPSK) modulation. With proper demodulation, the information content is detectable in the presence of overlaid ATCRBS signals. The downlink transmission modulation from the transponder is pulse position modulation (PPM), which is inherently resistant to ATCRBS random pulses. The information content for both uplink and downlink transmissions are further protected by parity check bits generated by a cyclic coding algorithm.

Each Mode S interrogation contains a 24-bit discrete address that allows a large number of aircraft to operate in the air traffic control environment without occurrence of a redundant address. The overlaying of the parity check bits on the discrete address assures the message will be accepted only by the aircraft addressed and minimizes the probability of an erroneous message being accepted.

(3) Basic System Protocol

The transponder equipped aircraft enters the airspace served by a Mode S interrogator and receives an ATCRBS/Mode S All-Call interrogation, having a waveform that solicits replies from both ATCRBS and Mode S transponders. ATCRBS transponders reply with a standard ATCRBS reply format, while Mode S transponders reply with a Mode S format including the discrete (24-bit) Mode S address. The address and location of the Mode S aircraft, is entered into a file (put on roll-call). On the next scan the Mode S equipped aircraft is discretely addressed. All aircraft on roll-call are interrogated according to a schedule computed from the azimuth and range of each aircraft. Within this schedule are ATCRBS/Mode S All-Calls that permit the tracking of known ATCRBS aircraft and the acquisition of additional ATCRBS and Mode S aircraft entering the served airspace.

Squitters are Mode S All-Call replies sent, by the aircraft, approximately once every second to inform anyone in the receiving airspace, the presence of a Mode S aircraft. Squitters trigger the interrogation process from ground interrogators for regular surveillance and other aircraft with airborne collision avoidance systems (ACAS).

(4) Mode S Message Content

All discrete Mode S interrogations (56-bit or 112-bit) and replies (except the All-Call reply) contain the 24-bit discrete address of the Mode S transponder. The discrete address is overlaid with 24 error-detecting parity check bits. In the All-Call reply, the 24 parity check bits are overlaid on the address of the Mode S interrogator and the discrete address of the transponder is included in the clear in the text of the reply.

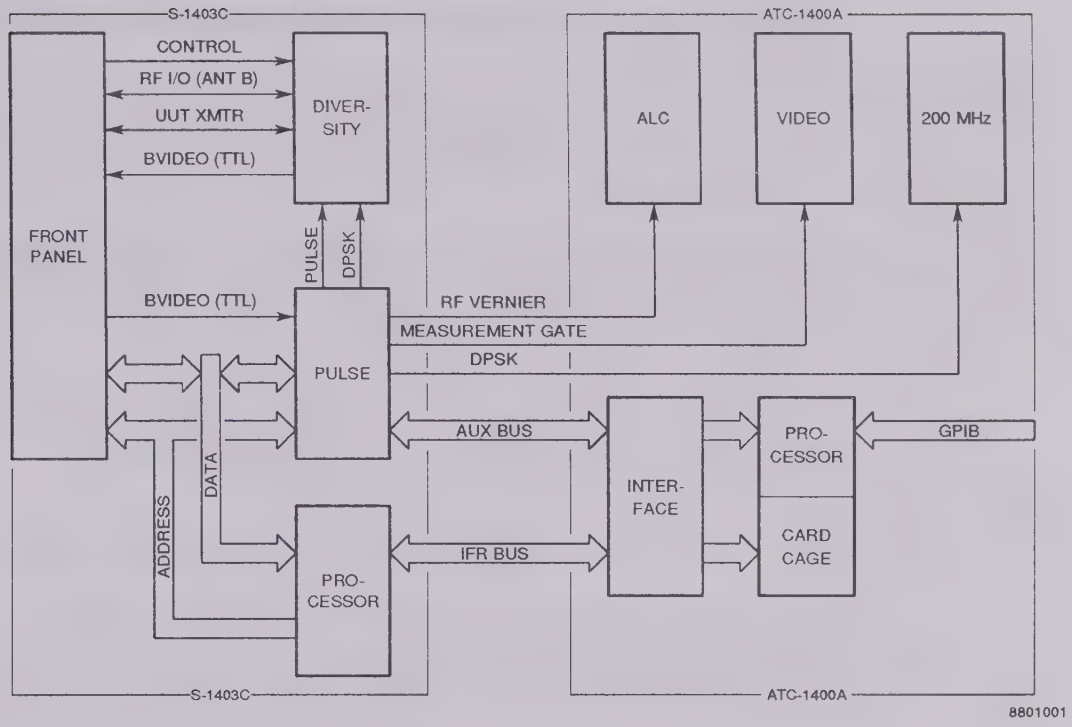
Discrete addressing and digital encoding allow Mode S transmissions to be used as digital data links. The interrogation and reply formats of the Mode S system contain sufficient coding space for transmission of data. The data transmissions are used for air traffic control purposes, collision avoidance or flight advisory services (i.e. weather reports, Automated Terminal Information System [ATIS], etc.).

C. System Theory of Operation (Refer to 2-2-1, Figure 1.)

(1) General

The Mode S Test System is a Ground Station Simulator, functioning as Air Traffic Control, transmitting and receiving air-to-air, ground based and other appropriate signals associated with Mode S.

The S-1403C receives and transmits all seven specifically defined Mode S formats corresponding to RTCA specification DO-181; Mar 1983. The Mode S signal is comprised of an 8 µs preamble and a 56 or 112 µs data block.




Mode S System Block Diagram
Figure 1

(2) S-1403C to ATC-1400A Communications

(a) Mode S Test System S-1403C to ATC-1400A Interface Definition

The outer 25-pin ribbon cable between the S-1403C, J10010 and ATC-1400A, J9102 (Auxiliary Bus) is used to transmit the high speed clock (20 MHz), pulse and video information from the ATC-1400A to the S-1403C. The S-1403C uses the clock input to generate pulses for interrogations transmitted through Antenna A (ATC-1400A RF I/O Connector) and Antenna B (ANT B Connector). The S-1403C uses the reply video information from Antenna A, to measure reply pulse parameters. The ATC-1400A also provides a synchronization signal called Self Interrogation (Self Interr), driven by the ATC-1400A PRF generator. Self Interr initiates test functions unless the EXT SYNC IN control has been turned on. ATC-1400A SLS enable gate control by the S-1403C is accomplished through the Auxiliary Bus.

The 25-pin ribbon cable between the S-1403C, J10011 and ATC-1400A, J9105 (IFR Bus) allows the two units to transfer control and data information. After power-on and each unit has performed an initialization sequence, the S-1403C transmits (to the ATC-1400A) the control output and data input locations within the ATC-1400A, the S-1403C override and monitor. Until power is removed, the S-1403C maintains primary control over the selected ATC-1400A functions. The IFR Bus also allows ASCII GPIB commands to be relayed to the S-1403C for execution and relays return data back to the ATC-1400A GPIB interface.

The S-1403C uses three separate coaxial cables to control the following ATC-1400A functions:

- An analog signal from the Pulse PC Board Assembly through the RF VERNIER OUT Connector (J10013) to the ATC-1400A Modulator through the RF LEVEL INPUT Connector (J9104) adjusts Antenna A RF Level ±3 dB.

- DPSK modulation from the Diversity Module through the DPSK OUT Connector (J10015) goes to the ATC-1400A Phase Modulator through the DABS INPUT Connector (J9101) for DPSK transitions in Antenna A Mode S interrogations.

- A gating control signal from the Pulse PC Board Assembly through the MEASUREMENT GATE OUT Connector (J10014) enables the ATC-1400A power meter circuit through the EXTERNAL MEASUREMENT GATE Connector (J9103).

(b) Mode S Test System S-1403C to ATC-1400A Interface Operation

The ATC-1400A continuously monitors the S-1403C through the IFR Bus. The ATC-1400A queries the S-1403C and looks for INTA (J10011-22) to be high and INTR (J10011-23) to be low. This is the initial state for the S-1403C and notifies the ATC-1400A to begin receiving data from the S-1403C.

The S-1403C receives data from the ATC-1400A when WRITE (J10011-17) is high and READ (J10011-20) is low. The ATC-1400A starts data transfer after the S-1403C sets both INTA and INTR high.

D. Functional Theory of Operation

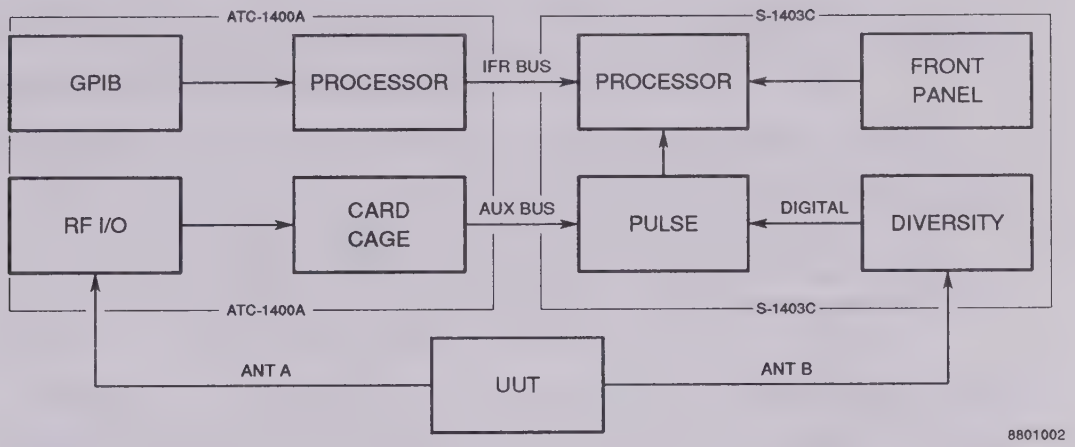
Functional theory concerning the operation of the Mode S Test System requires familiarity with the functional theory in the ATC-1400A Maintenance Manual.

(1) Introduction

The S-1403C Test Auxiliary provides pulse code modulation, when interfaced with the ATC-1400A Transponder/DME Test Set, for the purpose of testing ATC Mode-S Transponders. The S-1403C is operated manually using front panel controls and switches, or remotely by Automatic Test Equipment (ATE) control through the General Purpose Interface Bus (GPIB) Connector on the ATC-1400A.

The three functions associated with the Mode S Test System are Receive, Transmit and Test Validity.

(2) Receive (Refer to 2-2-1, Figure 2.)



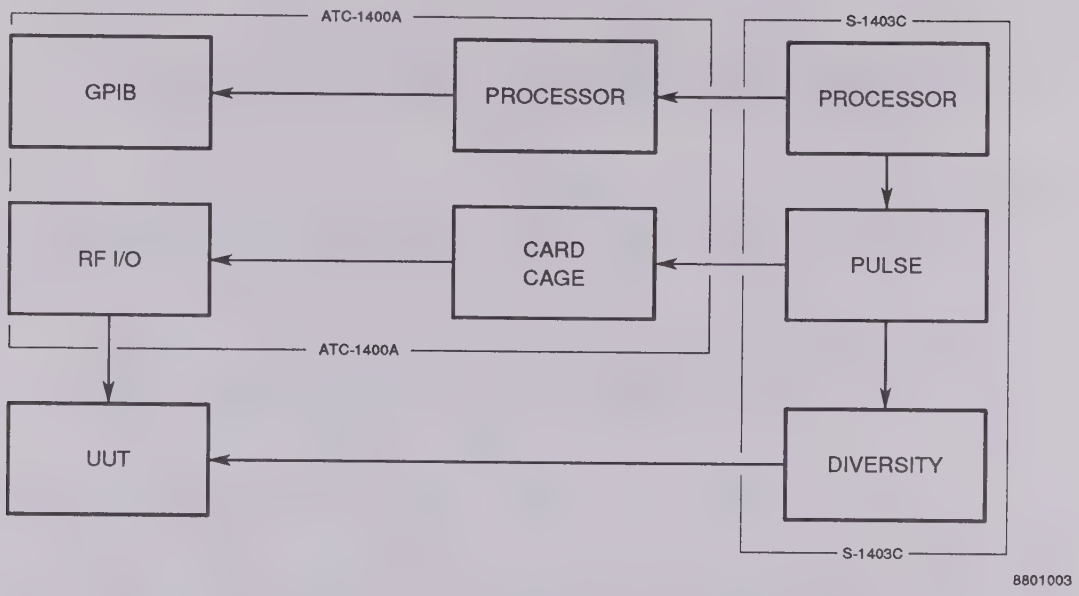

System Receive Block Diagram
Figure 2

The S-1403C receives information from the Keyboard on the face of the front panel, the Auxiliary Bus connected to the ATC-1400A or the UUT through the ANT B Connector.

Information from the Keyboard is sent to the Front Panel Processor PC Board Assembly where it is processed according to the format selected in the S-1403C menus. The main processor, on the Processor PC Board Assembly, receives the data and begins programming the pulse generator, on the Pulse PC Board Assembly, for the proper signal format.

The UUT transmits to the S-1403C through the ATC-1400A via the Auxiliary Bus (Antenna A) or the ANT B Connector (Antenna B). The Diversity Module demodulates the UUT signals. The Pulse PC Board Assembly decodes the resulting reply data.

(3) Transmit (Refer to 2-2-1, Figure 3.)




System Transmit Block Diagram
Figure 3

Data from the S-1403C is sent to the UUT from one of three locations; the ATC-1400A functioning as an L-Band Transmitter for ATCRBS interrogations, the Pulse PC Board Assembly utilizing signals programmed by the Processor PC Board Assembly for Modes S interrogations and the Diversity Module functioning as a second L-Band Transmitter providing both Mode S and ATCRBS interrogations according to formats specified by the Processor PC Board Assembly.

The ATC-1400A utilizes normal testing procedures for ATCRBS responses. Procedures are covered in the ATC-1400A Operation Manual. When replying to Mode S, the ATC-1400A transmits data according to instructions received from the S-1403C through the Auxiliary Bus.

The Pulse PC Board Assembly is programmed by the Processor PC Board Assembly. When prepared to interrogate, the S-1403C uses formats assigned by the Processor PC Board Assembly.

The Diversity Module operates as a second L-Band Transmitter to the ATC-1400A for transponders operating a second antenna (Antenna B). The Diversity Module provides delayed responses required for the second antenna, simulating the deviation between upper and lower antennas located on the aircraft. Without MLD, Antenna B level is fixed. With MLD installed, Antenna B level is adjustable. The diversity signal is sent to the UUT from the Diversity Module through the ANT B Connector on the S-1403C front panel.

(4) Test Validity

Mode-S transponder operation is validated with timing diagrams, located in the Mode S Test System Operation Manual, and by various indicators on the S-1403C and ATC-1400A front panels.

The S-1403C displays UUT reply delay (***RpDly:*** Field, Control Menu #1), percent reply (***%Reply:*** Field, Control Menu #1), squitter interval (***Sqtr:*** Field, Control Menu #1), squitter address (***Sqtr. Add.*** Field, Control Menu #2) and Mode S reply content (Sequence Menus). The ATC-1400A displays UUT transmit frequency (XMTR FREQ MHz Display), ATCRBS reply content (DISPLAY SELECT Readout) and pulse power (XMTR PWR WATTS Display). Displayed digital values provide easy reference against established parameters for the function being tested.

The Mode S Test System (ATC-1400A and S-1403C) validates the accuracy of data transferred between the UUT and Air Traffic Control. Together the S-1403C and ATC-1400A provide the L-Band signals necessary to simulate the ATC environment.

The GPIB provides remote operation capability for programmed testing configurations. Instructions are received through the IFR Bus. All actions normally performed by the front panel and ATC-1400A can be initiated through the GPIB.

E. Module Theory of Operation

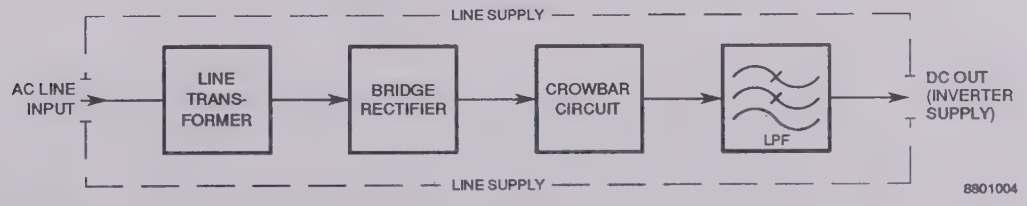
In addition to the block diagrams, refer to the appropriate circuit schematics in 2-2-3.

(1) Power Supply

The Power Supply consists of:

Line Supply PC Board Assembly
Inverter Supply PC Board Assembly
Power Distribution PC Board Assembly

(a) Line Supply PC Board Assembly (Refer to 1-2-1, Figure 4.)




Line Supply PC Board Assembly Block Diagram
Figure 4

The Line Supply PC Board Assembly is an ac to dc converter containing a power transformer, bridge rectifier and filter.

The AC IN Connector on the rear panel is connected to the front panel through P10015. T19001 has two primary windings connected in parallel when 115 VAC is selected by S10001 or in series if 230 VAC is selected. The secondary winding of T19001 is connected to a full wave rectifier BR19001, mounted on the side panel heat sink. C19001 and C19002 filter out the ripple from the +16 Vdc (nominal). Unregulated voltage from BR19001 is applied to Q19001 and the crowbar circuits.

Voltage, with most of the ripple removed, from Q19001 is applied through the Power Distribution PC Board Assembly to the Inverter Supply PC Board Assembly.

The crowbar circuit includes CR19003, R19002, R19003 and Q19002. If voltage becomes excessive, Q19002 will turn on, effectively shorting the bridge output causing the fuse (F10002) to open. F10002 opens when the line reaches approximately 160/320 VAC.

(b) Inverter Supply PC Board Assembly (Refer to 1-2-1, Figure 5.)

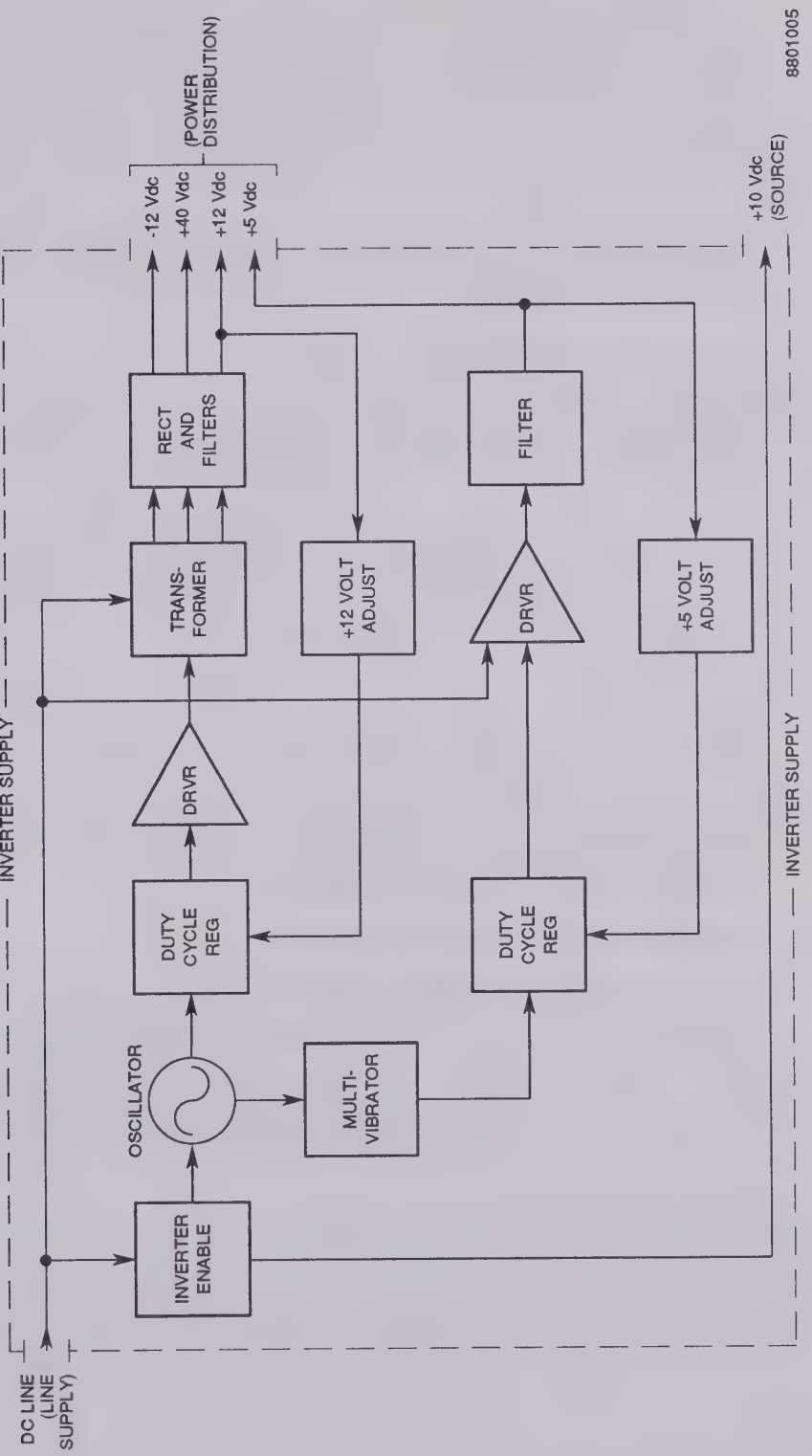
The Inverter Supply PC Board Assembly, part of the Power Supply Assembly, is a dc to dc flyback furnishing the ±12 Vdc, +40 Vdc, dc to dc back converter and filter for the +5 V.

The Inverter Supply PC Board Assembly contains a duty cycle regulator, transformer and rectifier circuit producing the regulated +12 Vdc, +40 Vdc and -12 Vdc distributed throughout the Test Set. The inverter supply voltage from the Line Supply PC Board Assembly is +12 to +24 Vdc, depending upon the line voltage.

Q17001 conducts a constant current, allowing +10 Vdc, set by Zener diode CR17004, to supply power to operate amplifiers U17001, U17002, U17003, U17005, U17006 and U17007. U17001 produces and applies a sawtooth output at approximately 45 kHz to the non-inverting input of U17002.

Zener diode CR17006, R17017 and R17015 set a voltage reference for the inverting input of integrator U17003. Feedback from the +12 Vdc secondary winding of T17001 is rectified by CR17011. Resistors R17018, R17019 and the +12V ADJUST R17020 set the voltage compared with the reference voltage by U17003. L17003 and C17009 smooth out the ripples in the +12 Vdc output.

U17002 compares the oscillator ramp with the feedback from U17003 and produces a pulsed output whose duty cycle decreases as the integrated feedback voltage increases. R17010 sets a maximum duty cycle of 50%. The high output from U17002 turns on Q17003, applying voltage to the gate of Q17005. Q17005 conducts, pulling current through the primary winding of T17001. When U17002 output goes low, Q17003 is turned off, and Q17004 is turned on. Q17005 shuts off and current through T17001 is reduced. The building up and collapsing of the magnetic winding of T17001 is directly related to the duty cycle of U17002.




Inverter Supply PC Board Assembly Block Diagram
Figure 5

Total current induced into the secondary windings is proportional to the magnetic flux developed during the duty cycle of U17002. The +40 Vdc and -12 Vdc supplies track the +12 Vdc supply. As the total load varies, U17003 integrates the error voltage and raises or lowers the duty cycle accordingly. Increasing the load increases the duty cycle, which increases the transfer of power from the primary winding of T17001 to the secondary windings.

The flyback currents from the secondary windings are half-wave rectified by individual diodes. The +40 Vdc supply is RC-filtered; the other supplies are LC-filtered.

The +5 Vdc is produced by a back converter consisting of Q17008 in parallel with Q17010, CR17013, L17007 and C17014. The input dc voltage (+16 V) is applied to L17007 during a portion of the cycle through Q17008 and Q17010. During the remainder of the cycle (the OFF portion), the current through L17007 is supplied through CR17013.

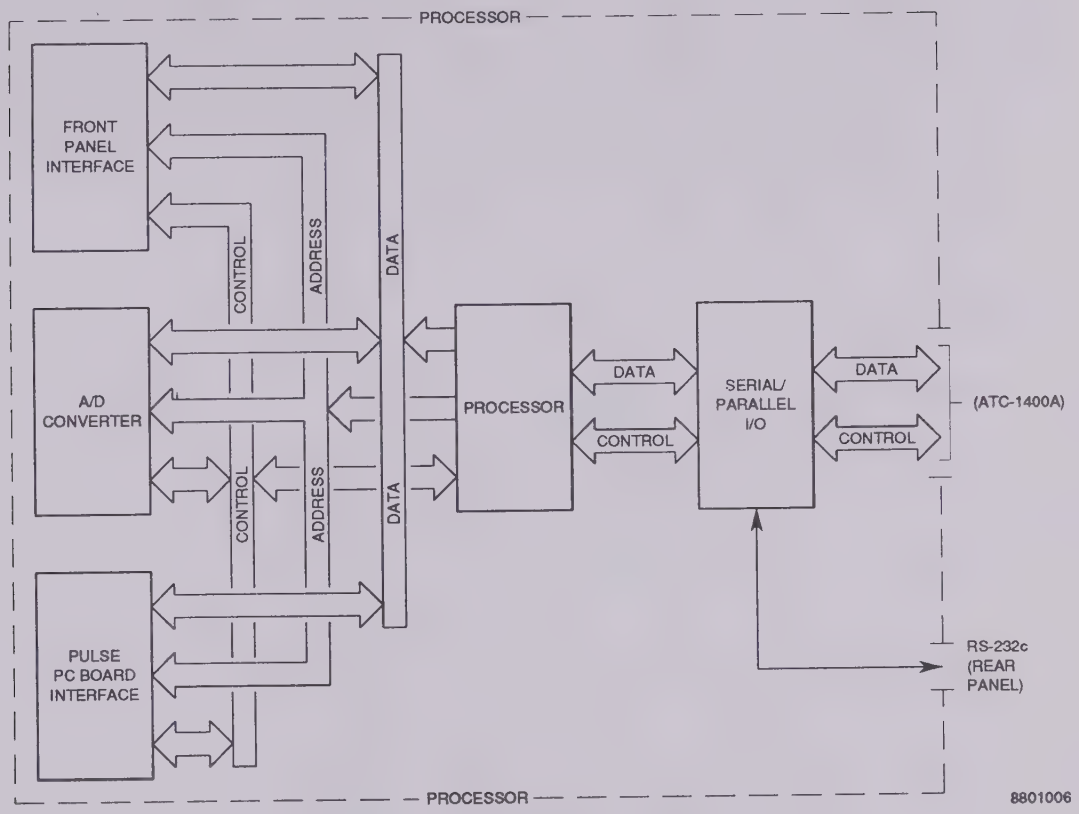
A ramp voltage is applied to pin 3 of U17006 by charging C17013 through R17024. Pin 10 of U17005 goes high to charge C17013 creating the ramp voltage. U17005 is triggered by the 45 kHz oscillator U17001, causing the +5 V regulator and the +12 V regulator to alternately pull on the +16 V supply line. By alternating in this manner, ripple current is decreased on the supply line.

Integrator U17007 compares the fixed dc reference to the feedback voltage from C17014. U17006 sets the duty cycle for the +5 V regulator by comparing the integrated error voltage from U17007 with the ramp voltage. When Q17009 is off, FETs Q17008 and Q17010 are held on by Q17006. When Q17009 is on, the FETs are turned off through Q17007. R17035, R17036 and the +5V ADJUST R17037 set the feedback voltage, compared with the reference voltage by U17007.

(c) Power Distribution PC Board Assembly

Power Distribution PC Board Assembly is mounted on the Power Supply Assembly and contains the +12 Vdc regulator which supplies the front panel power indicator and cooling fan. The +16 Vdc, from the Line Supply PC Board Assembly, is applied to the +12 Vdc regulator U18001. VCXO ADJ R16003 sets the voltage applied to the TCXO, part of the Diversity Module, to maintain the 10 MHz internal reference frequency.

(2) Processor PC Board Assembly (Refer to 1-2-1, Figure 6.)




Processor PC Board Assembly Block Diagram
Figure 6

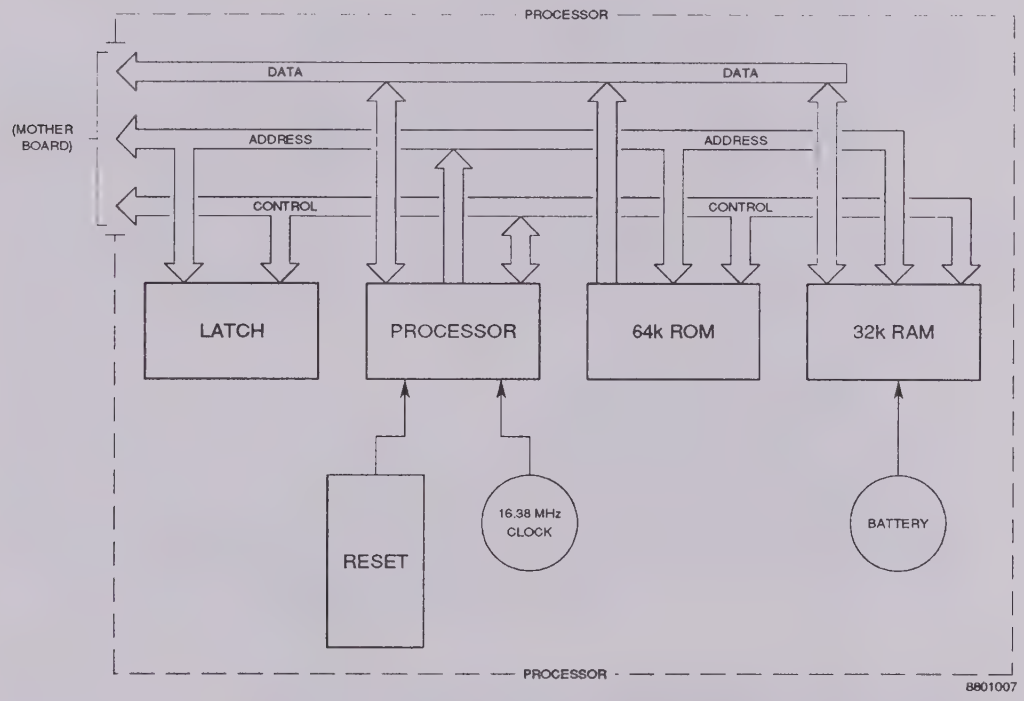
The Processor PC Board Assembly consists of:

Processor/System Memory
Serial/Parallel I/O
Analog to Digital (A/D) Converter
Front Panel Interface
Pulse PC Board Interface

The Processor PC Board Assembly is the data control center between the front panel, Pulse PC Board Assembly and ATC-1400A. Control is accomplished through use of 128 kbytes of operating memory and high integration 8-bit microprocessor. All external interactions are buffered to prevent unwanted signals from entering the Processor section. A +3 Vdc Battery prevents memory loss in the absence of applied power.

The Processor PC Board Assembly is given commands from the Front Panel Processor or the ATC-1400A processor with remote operation through GPIB. The Processor PC Board Assembly then: programs the Pulse PC Board Assembly according to the menu items selected by the operator on the Front Panel Display, generates control signals for the Diversity Module which is sent by way of the data bus through the front panel to the Diversity Module and determines for the Pulse PC Board Assembly whether to transmit or receive the various ATCRBS/MODE S formats.

(a) Processor/System Memory (Refer to 1-2-1, Figure 7.)




Processor/System Memory Block Diagram
Figure 7

Processor/System Memory has four major components: Microprocessor U12001, two 64k ROMs (U12002, U12009) and 32k RAM U12003. U12001, a multi-functional 80188 microprocessor, receives instruction data from the two 64k ROMs and carries out assignments as instructed. To accomplish this, U12001 has 10 chip selects. Refer to 2-2-1, Table 1 for chip select definition. Chip select lines are active low.

| CHIP SELECT | LINE | SELECTION | ADDRESSES |
|---|---|---|---|
| Upper | $\overline{UCS}$ | 64k ROM (U12002) | F0000-FFFFFh |
| Lower | $\overline{LCS}$ | 32k RAM (U12003) | 00000-08000h |
| Mid-range | $\overline{MCS1}$ | Pulse PC Board Assembly (U11011) | D0000-DFFFFh |
| | $\overline{MCS2}$ | 64k ROM (U12009) | E0000-EFFFFh |
| Peripheral | $\overline{PCS0}$ | Front Panel Assembly (U14001) | 400-47Fh |
| | $\overline{PCS1}$ | Serial-Parallel I/O (U12005) | 480-4FFh |
| | $\overline{PCS2}$ | Pulse PC Board Assembly (U11014) | 500-57Fh |
| | $\overline{PCS3}$ | A/D Converter (U14010B) | 580-5FFh |
| | $\overline{PCS5}$ | A/D Converter (U14017B) | 680-6FFh |
| | $\overline{PCS6}$ | Pulse PC Board Assembly (INTA-U11011) | 700-780h |

Microprocessor U12001 Chip Selects
Table 1

Instruction sequence:

- Address latch enable (ALE) line (U12001-61) to Transparent Latch U12004 goes high, allowing U12001 to set address where data is to be received through data lines to U12004.
- When address is valid, ALE goes low, causing the lower 8 bits of the address to be latched onto U12004 address lines, allowing U12001 to receive data on data lines without changing address selected.
- $\overline{UCS}$ line (U12001-34) is low to enable U12002. Read ($\overline{RD}$) line (U12001-62) goes low to enable data byte at address selected (initial address is FFFF0) to be sent to U12001.
- Data is processed and instruction is carried out in same fashion (ALE goes high, chip is selected, valid address is latched and data is read from or written to address). Write ($\overline{WR}$) line (U12001-63), instead of Read line, goes low when sending data to an address.

U12001 also provides Direct Memory Access (DMA) capabilities for the Pulse PC Board Assembly. DRQ0 (U12001-18) and DRQ1 (U12001-19) lines set up DMA, allowing a direct read or write to memory.

DMA sequence:

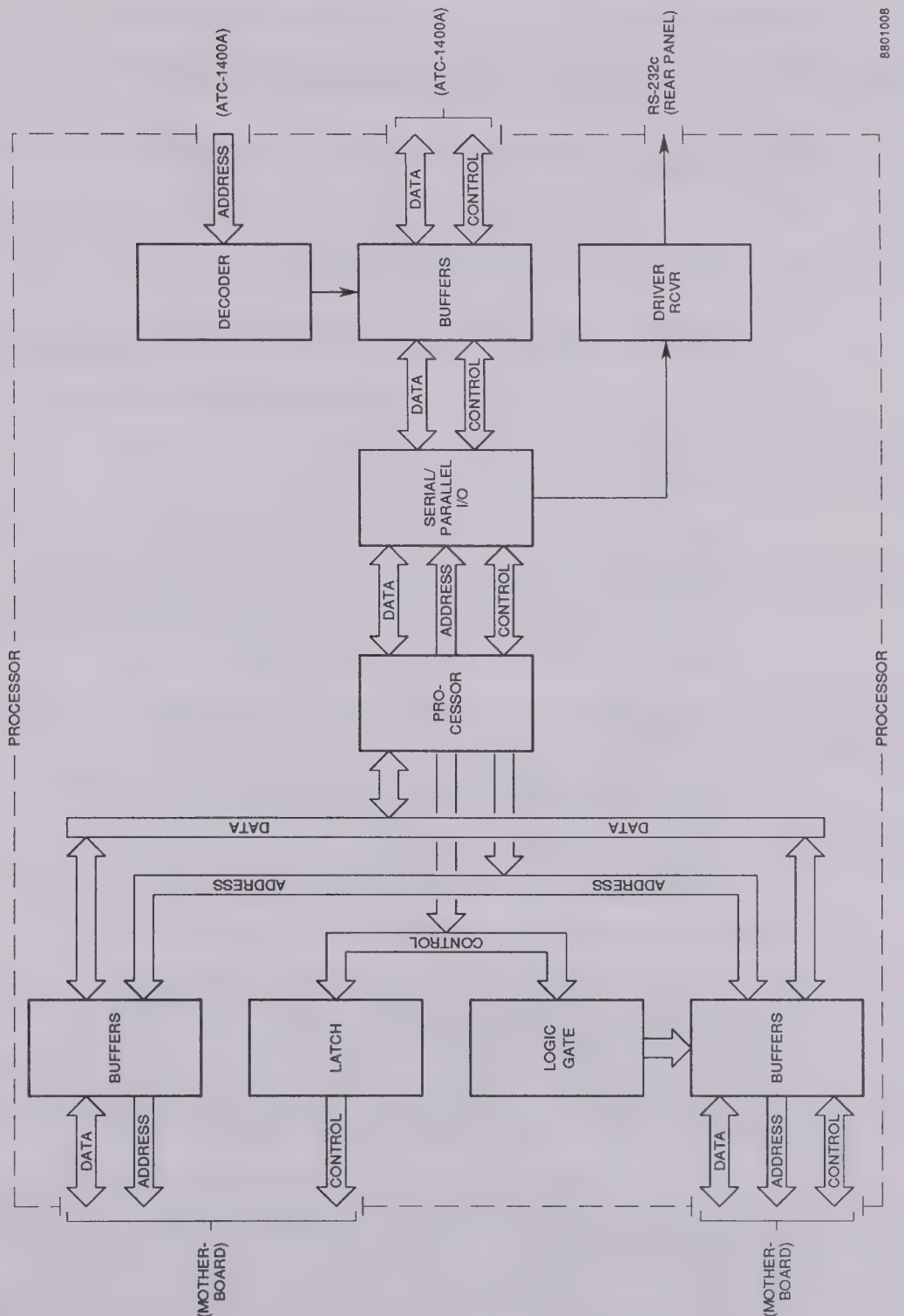
- DRQ0 (from Pulse PC Board Assembly, Reply Decoder) or DRQ1 (from Pulse PC Board Assembly, Edge Detector) goes high (DMA request).
- U12002 finishes current process.
- DMA takes control and programmed action is initiated.

There are three interrupt lines used on U12001. The signal PA2 from the Pulse PC Board Assembly indicates the Reply Decoder has detected an unsolicited Mode S DF11 reply (squitter) and causes U12005 of the Serial/Parallel I/O to interrupt U12001. INT0 (U12001-45) goes high from U12005, informing U12001, a data read is required. INT2 (U12001-42) is an active low handshake with U12005, acknowledging the read request. INT1 (U12001-44) is high when activated by the Pulse Generator on the Pulse PC Board Assembly.

Other circuits important to operation are timers, crystal, reset and battery back-up. U12001 provides two timers, T0 (U21001-22) used by U12005 and T1 (U12001-23) used by the Pulse PC Board Assembly. Crystal Y12001, with inputs at X1 (U12001-59) and X2 (U12001-58), provides the 16.384 MHz oscillation frequency that is divided by 2 (8.192 MHz) and used internally by U12001. On power up, U12022 resets U12001, verifies +5 Vdc is present and delays operation a few milliseconds (timed by C12005 discharge in conjunction with U12022) to allow Y12001 to get at full oscillation. Lithium Battery BT12001 provides +3 Vdc to the 32k RAM U12003 so data entered into memory is not lost when power is off. Q12001 and Q12002 form a differential amplifier that detects power-off conditions by monitoring the +5 V line. When the output of Q12001 goes below approximately +4.5 V (referenced by CR12003), Q12001 shuts off. Deactivating Q12001 shuts off Q12003, Q12005 and Q12004 to disable RAM select from U12001, preventing data in non-volatile RAM from being inadvertently changed. When the +5 V line drops below approximately +3 V, CR12004 becomes reverse biased and CR12005 becomes forward biased. When CR12005 is forward biased, BT12001 keeps RAM chip enable high, preventing any inadvertent memory transfer.

(b) Serial/Parallel I/O (Refer to 2-2-1, Figure 8.)

The Serial/Parallel I/O is used for RS-232 (serial) communication and parallel communication with the ATC-1400A (for GPIB operation). Driver/Receiver U12007 and Multifunction Universal Asynchronous Receiver-Transmitter (MUART) U12005 are used for RS-232 communication through J10012. U12005, Decoder U12008, Bi-Directional Buffer/Driver U12006, Tri-State Buffers (U12016A, U12016B) and Inverter U12015F are used for parallel communication through J10011.




Processor PC Board Communications Block Diagram
Figure 8

Serial sequence:

- U12007 converts serial data received on RXD (U12007-8) to a TTL level and sends it to U12005.
- U12005 converts the data to parallel with the start and stop bits removed.
- U12005 internally latches address from U12001 after request has been made. While $\overline{RD}$ and $\overline{PCS1}$ (U12001-27) are low, U12001 reads the data one character at a time.
- Transmit is accomplished in same fashion with $\overline{WR}$ and $\overline{PCS1}$ low. U12005 receives a low on $\overline{CTS}$ (U12005-21) indicating clear to send.
- U12005 converts parallel data to serial and sends it on TXD (U12005-23).

Parallel sequence:

- The ATC-1400A sends highs on A0 (J10011-2) and A1 (J10011-3), accompanied by lows on A2 (J10011-5) and A3 (J10011-8) to receive parallel data through J10011. U12008 decodes the data and Y3 output (U12008-12) goes low, activating U12016A and U12016B to setup handshake signals from U12005 to the ATC-1400A. U12015F output goes high, informing U12005 of data to read.
- U12005 sends a low on the read line setting U12006 up to receive incoming data.
- When U12005 is accessed at correct address, ATC-1400A sends data through U12006 and U12005 for U12001 to read.
- Transmit is the same in reverse except U12005 activates write line while keeping read line high to put U12006 in transmit mode.

(c) Analog to Digital (A/D) Converter

The A/D Converter provides the digital information used in temperature compensation, positioning the Synchronous Phase Reversal (SPR) and calculating reply delays. The A/D Converter section consists of a multiplexed Analog to Digital Converter U12011, D Flip-Flop U12010B, NOR gates (U12017B, U12017C), Inverter U12015C, Tri-State Buffer U12014C, Temperature Compensation Diode CR12002, Potentiometers (R12003, R12007, R12005, R12006) and R12002.

Temperature Compensation Diode CR12002, R12002 and the TEMP ADJ R12003 provide the input voltage (U12011-1) for temperature compensation. SPR TIMING Adjust R12007 sets the input voltage (U12011-3) for the coarse SPR position reference. (The Pulse PC Board Assembly provides the finer adjustments to maintain correct SPR position.) ANT A REPLY DELAY Adjust R12006 and ANT B REPLY DELAY Adjust R12005 set levels for calibrated reply delay measurements. U12011 sends converted data, one bit at a time, through the only output (U12011-16).

A/D Converter sequence:

- $\overline{PCS5}$ (U12001-31) and $\overline{WR}$ (U12001-63) go low. NOR gate U12017B output goes high to set U1210B Q output to low, selecting U12011.
- $\overline{RD}$ from U12001 goes low. NOR gate (U12017C) causes I/O CLK input (U12011-18) to go high, triggering data output. The high from U12017C is also inverted low by U12015C, turning on U12014C which allows data to be read by U12001.
- $\overline{RD}$ going low is repeated eight times to read the full eight bit conversion generated by U12011.
- $\overline{PCS3}$ (U12001-29) goes low to reset U12010B.

(d) Front Panel Interface

The Front Panel interface uses Bi-Directional Buffer U12013, Transparent Latch U12012, Tri-State Buffers (U12014A, U12014B, U12014D) and Resistive Networks (RN12001, RN12002, RN12003) to communicate with the Front Panel Assembly.

U12014A, U12014B and U12014D are used to drive control signals off the board while RN12001, RN12002 and RN12003 hold inactive lines to a high impedance state.

Front Panel Interface sequence:

- $\overline{PCS0}$ (U12001-25) goes low to request data. ALE goes high. When valid address is latched and buffered by U12012, ALE goes back low.
- When $\overline{RD}$ goes low, U12013 receives data for U12001 to read.
- Writing data is the same, only $\overline{WR}$ is low and $\overline{RD}$ is high, allowing U12001 to transmit data through U12013.

(e) Pulse PC Board Interface

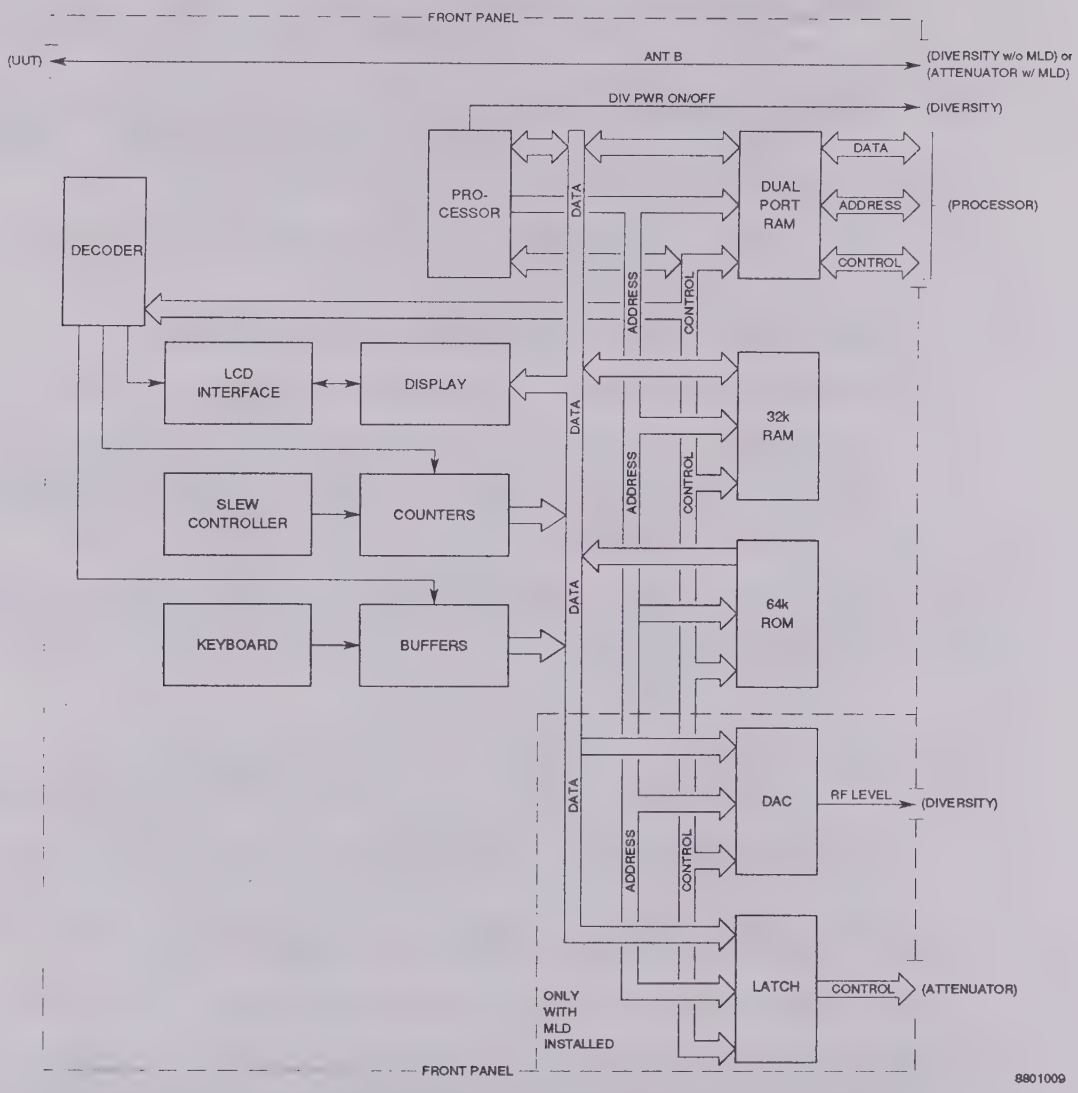
The Pulse PC Board Interface uses Tri-State Buffers (U12018, U12019, U12020), Inverters (U12015A, U12015B), NOR gate U12017A, Bi-Directional Buffer U12021 and Resistive Network RN12004 to communicate with the Pulse PC Board Assembly.

U12019 and U12020 drive address lines while U12018 drives control lines. RN12004 holds inactive control lines to a high impedance state.

Pulse PC Board Assembly Interface sequence:

- $\overline{PCS2}$ (U12001-28) or $\overline{MCS1}$ (U12001-37) goes low, is inverted to high by U12015 and back to low by U12017A. U12001 is activated.
- When $\overline{RD}$ is low, U12021 is set to receive data for U12001 to read.
- When $\overline{WR}$ is low, $\overline{RD}$ is high, allowing U12021 to buffer and transmit data from U12001 to the Pulse PC Board Assembly.

(3) Front Panel Assembly (Refer to 2-2-1, Figure 9.)




Front Panel Assembly Block Diagram
Figure 9

The Front Panel Assembly consists of:

Keyboard
Slew Controller
LCD Interface
Processor/Memory
Antenna B Level Control (only with MLD)

The Front Panel Assembly provides the interface between operator and S-1403C. This is accomplished through converting data from Keyboard and Slew Control to formatted data used in processing and updating the Display. Two connectors (ANT B and UUT XMTR) are provided to transmit and receive data between the UUT and the Diversity Module.

(a) Keyboard

The Keyboard consists of the Keyboard PC Board Assembly, Buffer/Drivers (U14012, U14008) and associated components found on the Front Panel Processor PC Board Assembly.

When the Keyboard is inactive, Resistive Networks (RN14001, RN14002) hold the row and column lines to a high impedance. When a key is pressed, a row and column line are connected together.

Keyboard sequence example:

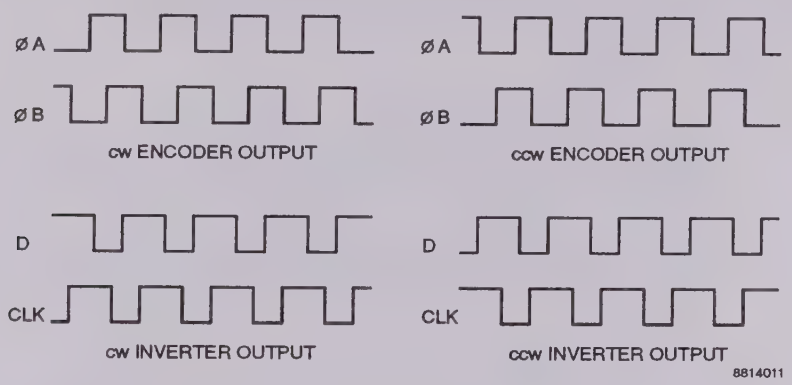
- Pressing the ← CURSOR Key connects row 1 with column 1. Circuit closes and current flows.
- Current flowing through the base, turns Q14004 on allowing the low ground on emitter through Diode CR14001 to Schmitt Trigger Inverter U14007F. The high output sends an interrupt (INT0, U14001-45) to Processor U14001.
- The low through Q14004 is also sent through U14012 when enabled by Decoder U14009. When A12, A14 and A15 are high with A13, $\overline{LCS}$ and ALE low (DXXXh address selected) from U14001; the output Y5 from U14009 becomes low activating U14012. D0 is then read low by U14001 indicating a key in column 1 was pressed.
- The low at R14010 and Q14004 is sent through U14008 when enabled by U14009. When A14 and A15 are high with A12, A13, $\overline{LCS}$ and ALE low (CXXXh address selected) from U14001; the output Y4 from U14009 becomes low activating U14008. D0 is read low again by U14001 indicating the key pressed in column 1 was also in row 1.

The Diversity Module installed line is read through U14008 when addressed through U14009. If D7 is high, Diversity Module is not installed.

(b) Slew Controller

The Slew Controller processes and modifies information for data input to the Processor PC Board Assembly. The Slew Controller includes Rotary Encoder RE15001 on Front Panel Assembly and D Flip-Flops (U14015A, U14015B), Counters (U14011, U14014), Buffer/Driver U14013 and associated components on the Front Panel Processor PC Board Assembly.

RE15001, when rotated, generates two square wave signals labeled ϕA and ϕB, 90° out of phase. Refer to 2-2-1, Figure 10. Slew Control is based upon two factors, whether ϕA or ϕB is leading phase and how many clock counts occur in the adjustment process.




Slew Control Timing Diagram
Figure 10

Slew Control sequence:

- RE15001 is rotated. When increasing the count, direction is clockwise (cw) and ϕA leads ϕB. When decreasing the count, direction is counterclockwise (ccw) and ϕB leads ϕA.
- ϕA and ϕB are inverted by Schmitt Trigger Inverters U14007A and U14007B respectively.
- While D is high, the rising edge of CLK sets the D Flip-Flop U14015A outputs Q to high and $\overline{Q}$ to low. While D is low, the rising edge of CLK sets U14015A outputs Q to low and $\overline{Q}$ to high.
- With $\overline{Q}$ low, cascading Counters U14014 and U14011 are set to count up. With $\overline{Q}$ high, U14014 and U14011 are set to count down.
- U14014 counts up or down from 80h one count every time CLK goes high. When U14014 is full, RC output goes low then back high on next rising edge of CLK. U14014 is reset and starts counting again while U14015 counts every time RC goes high.
- Count (U14014 with lower byte and U14015 with upper byte) is sent through Buffer/Driver U14013 when enabled by U14009. When A13 and A15 are high with A12, A14, $\overline{LCS}$ and ALE low (AXXX address selected) from U14001; Y2 output from U14009 becomes low activating U14013. U14013 is read by U14001 every 50 ms.
- If maximum (FFh) or minimum (00h) count is reached, both counters send a high input to two NAND gates (U14010C and U14010D) in series, effectively forming an AND gate with a high output that disables counters (through $\overline{G}$ input).

Counters are reset when changing directions on RE15001 or when instructed by U14001.

On the rising edge of CLK, Q output of U14015A is identical to the Q output of U14015B. When RE15001 has a direction change, the last Q state is momentarily felt at the output of U14015B (until next CLK rising edge) while Q output from U14015A changes. XOR gate U14016A goes high and NOR gate U14006A goes low, resetting the counters back to 80h.

U14001 clears counters with address BXXX. When A12, A13 and A15 are high with A14, $\overline{LCS}$ and ALE low to U14009; Y3 output goes low causing XOR gate U14016D to go high. U14006A goes low, resetting counters back to 80h.

(c) LCD Interface

The LCD Interface provides the display and lighting controls for the Front Panel Display.

Display data control is accomplished by the Processor U14001, Decoder U14009, NOR gates (U14006B, U14006C and U14006D) and NAND gate U14010B.

LCD Interface sequence:

- Read ($\overline{RD}$) or Write ($\overline{WR}$) line goes low causing outputs of U14010B to go high and U14006B to go low.
- $\overline{LCS}$ and ALE are low with A15 is high to enable U14009.

  When A12, A13 and A14 are low; U14009 Y0 output is low causing output of U14006D to be high (only when RD or WR is low), activating top half of display (E1 through J14003).

  When A12 is high with A13 and A14 low, U14009 Y1 output is low causing output of U14006C to be high (only when RD or WR is low), activating bottom half of display (E2 through J14003).
- A0 and A1 control data action to the display. Refer to 2-2-1, Table 2 for definition.
- Data is transferred over data lines between U14001 and display.

Display backlighting is controlled through Variable Resistor R15001. When R15001 is rotated clockwise, resistance through R15001 and R14015 is increased , causing the base of Transistor Q14005 to have a higher positive potential. Q14005 allows more current to pass through R14011, Q14005 and Inverter Transformer T14001. T14001 converts dc input to high voltage ac output. As current increases, backlighting brightness on front panel display increases. R14013, R14014 and CR14006 provide the necessary voltage drop used in driving the Liquid Crystal contrast control.

| SELECTED ADDRESS | ADDRESS LINES | | | | | | ACTION/REGISTER | DISPLAY SECTION |
|---|---|---|---|---|---|---|---|---|
| | A15 | A14 | A13 | A12 | A1 | A0 | | |
| 8XX0 | 1 | 0 | 0 | 0 | 0 | 0 | Write/Instruction Register | Top |
| 8XX1 | 1 | 0 | 0 | 0 | 0 | 1 | Write/Data Register | Top |
| 8XX2 | 1 | 0 | 0 | 0 | 1 | 0 | Read/Instruction Register (Busy Flag) | Top |
| 8XX3 | 1 | 0 | 0 | 0 | 1 | 1 | Read/ Data Register | Top |
| 9XX0 | 1 | 0 | 0 | 1 | 0 | 0 | Write/Instruction Register | Bottom |
| 9XX1 | 1 | 0 | 0 | 1 | 0 | 1 | Write/Data Register | Bottom |
| 9XX2 | 1 | 0 | 0 | 1 | 1 | 0 | Read/Instruction Register (Busy Flag) | Bottom |
| 9XX3 | 1 | 0 | 0 | 1 | 1 | 1 | Read/ Data Register | Bottom |

LCD Control
Table 2

(d) Processor/Memory

The Processor/Memory section on the Front Panel Processor PC Board Assembly provides direct communication and data transfers between the Processor PC Board Assembly and Front Panel Controls.

Processor/Memory consists of Microprocessor U14001, Transparent Latch U14002, 64k ROM U14003, 32k RAM U14004 and Dual Port RAM (DPR) U14005. Crystal Oscillator Y14001 resonates at 11.059 MHz, providing the input used by U14001 for internal timing. U14018 works in conjunction with C14027 to delay operation on power up, allowing Y14001 to be at correct operating frequency. Diversity Module power is controlled by D Flip-Flop U14017. On rising edge of $\overline{PCS0}$ (U14001-25), if D0 is high, Diversity Module power turns off. If D0 is low, Diversity Module power turns on.

U14001 is an 80188 microprocessor and operates identically to U12001 on the Processor PC Board Assembly. Transparent Latch U14002 latches lower byte addresses, allowing address lines to be used for addresses and data. 32k RAM U14004 is selected when $\overline{LCS}$ and A15 are low causing Schmitt Trigger Inverters (U14007C, U14007D) to go high. This causes NAND gate U14010A to go low enabling U14004. DPR U14005 is accessed by either U14001 or U12001. U14001 accesses U14005 through U14009 at address EXXX. When A12, $\overline{LCS}$ and ALE are low with A13, A14 and A15 high from U14001; Y6 output from U14009 is low to enable left port of U14005. A high on INT1 (U14001-44) informs U14001 that the Processor PC Board Assembly has either loaded or requested information through U14005. When U14005 is accessed, a busy signal (U14005-3 and 45) is sent to the appropriate processor (U14001 or U12001) to prevent address conflicts.

(e) Antenna B Level Control (only with MLD)

When the MLD option is installed, the Front Panel Processor PC Board Assembly controls the signal level through the ANT B Connector. U14001 sets the Antenna B RF level from information entered into ***Brf=*** Field in Control Menu #2. U14001 sends data (01h to 7Bh) through D Flip-Flop U14017, accessed when $\overline{PCS0}$ is low, to control step attenuator on the Attenuator Assembly. Actual attenuation is offset by 20 dB, due to signal level output from the Diversity Module, to provide the specified -20 to -80 dBm range.

Decoder U14020, 10-Bit Digital to Analog Converter (DAC) U140021 and associated components provide for Antenna B RF vernier operation. U14001 uses the value from the ***BrfIvl=*** Field in Control Menu #2 to adjust Antenna B level.

Antenna B RF Vernier sequence:

- $\overline{PCS1}$, ALE and $\overline{WR}$ lines go low to access Decoder U14020. $\overline{WR}$ is inverted through Schmitt Trigger Inverter U14007E.
- Address lines A0, A1 and A2 are low to set U14020 Y0 output low and activate first chip enable line to DAC U14021.
- U14001 sends the first eight data bits, using D0 to D7 data lines, to U14021.
- Address line A0 goes high with A1 and A2 lines low to set U14020 Y1 output low and activate second chip enable line to DAC U14021.
- U14001 sends the last two data bits using D0 to D1 data lines (D8 and D9 on U14021) to U14021.
- U14021 converts the data to an analog voltage (U14021-20) to drive the EXT AM MOD input to the Diversity I/O PC Board Assembly.

Refer to 2-2-1, Table 3 for Antenna B RF vernier according to DAC input value. R14021 calibrates the output current to maintain the specified ±3.0 dB Antenna B RF vernier range.

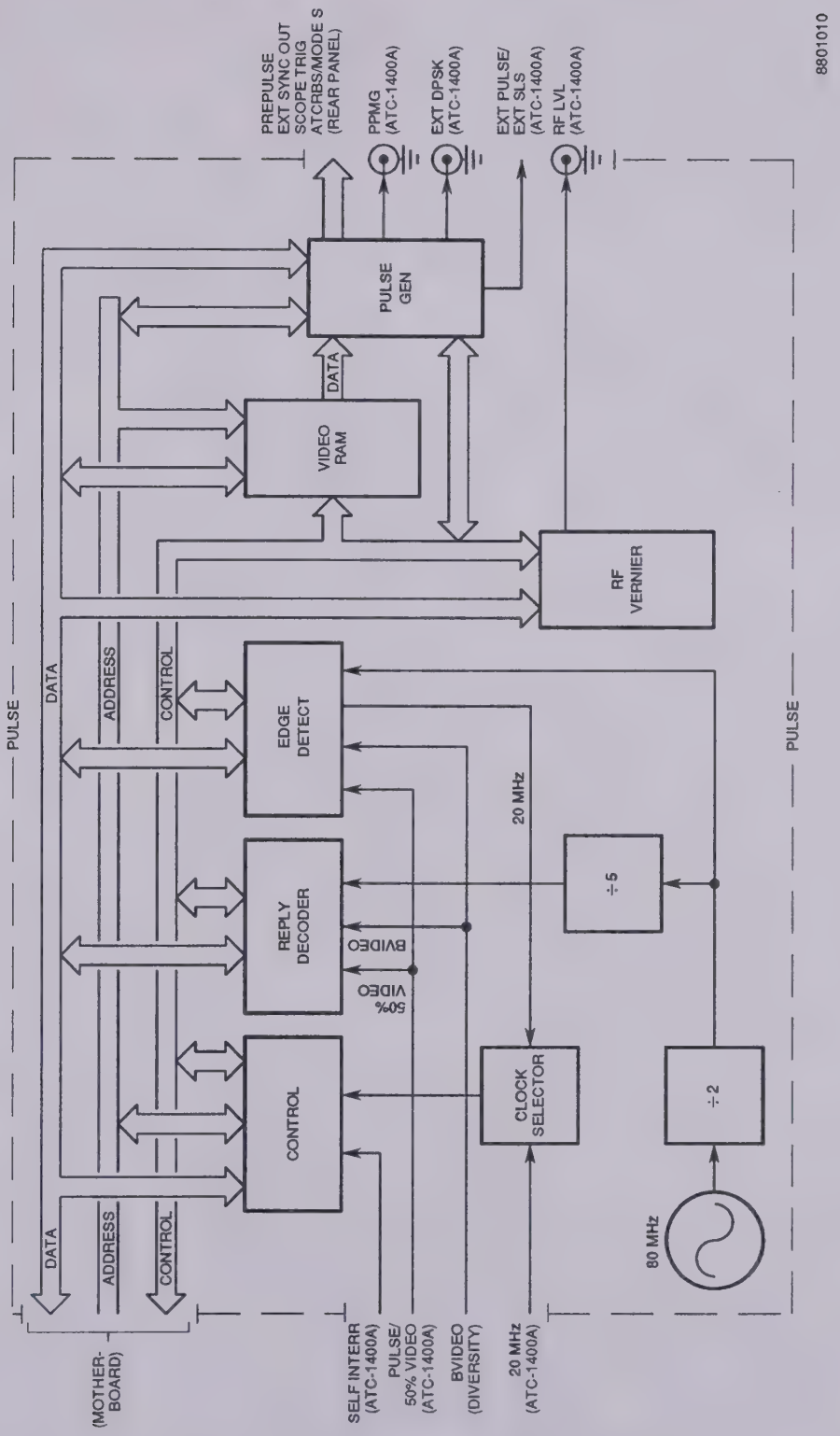
| VERNIER (dB) | DAC INPUT (h) | VERNIER (dB) | DAC INPUT (h) | VERNIER (dB) | DAC INPUT (h) |
|---|---|---|---|---|---|
| -3.0 | 27 | -0.9 | 118 | 1.1 | 253 |
| -2.9 | 2F | -0.8 | 126 | 1.2 | 263 |
| -2.8 | 3A | -0.7 | 134 | 1.3 | 276 |
| -2.7 | 45 | -0.6 | 141 | 1.4 | 28A |
| -2.6 | 4F | -0.5 | 14F | 1.5 | 29A |
| -2.5 | 5A | -0.4 | 15D | 1.6 | 2B1 |
| -2.4 | 66 | -0.3 | 168 | 1.7 | 2C5 |
| -2.3 | 70 | -0.2 | 17A | 1.8 | 2D6 |
| -2.2 | 7E | -0.1 | 18A | 1.9 | 2E9 |
| -2.1 | 88 | 0.0 | 19A | 2.0 | 2FD |
| -2.0 | 95 | 0.1 | 1AA | 2.1 | 310 |
| -1.9 | A0 | 0.2 | 189 | 2.2 | 326 |
| -1.8 | AC | 0.3 | 1C0 | 2.3 | 33C |
| -1.7 | B8 | 0.4 | 1DC | 2.4 | 350 |
| -1.6 | C5 | 0.5 | 1EB | 2.5 | 365 |
| -1.5 | D0 | 0.6 | 203 | 2.6 | 37C |
| -1.4 | DA | 0.7 | 211 | 2.7 | 38E |
| -1.3 | E4 | 0.8 | 221 | 2.8 | 3A3 |
| -1.2 | F0 | 0.9 | 234 | 2.9 | 3BD |
| 1.1 | FE | 1.0 | 244 | 3.0 | 3CE |
| -1.0 | 10A | | | | |

Antenna B RF Vernier
Table 3

(4) Pulse PC Board Assembly (Refer to 2-2-1, Figure 11.)

The Pulse PC Board Assembly consists of:

Pulse Generator
Edge Detect
Reply Decoder
Control
RF Vernier




Pulse PC Board Assembly Block Diagram
Figure 11

The Pulse PC Board Assembly provides pulses and DPSK information used to modulate outgoing interrogation signals. The Pulse PC Board Assembly also monitors and decodes pulse information and controls several functions.

The Pulse PC Board Assembly receives instructions from the Microprocessor U12001 on the Processor PC Board Assembly through the data and address lines. Different operations are accomplished efficiently with the use of four XILINX Logic Cell Array (LCA) components. LCAs incorporate several circuits internally to accomplish the various functions.

(a) Pulse Generator

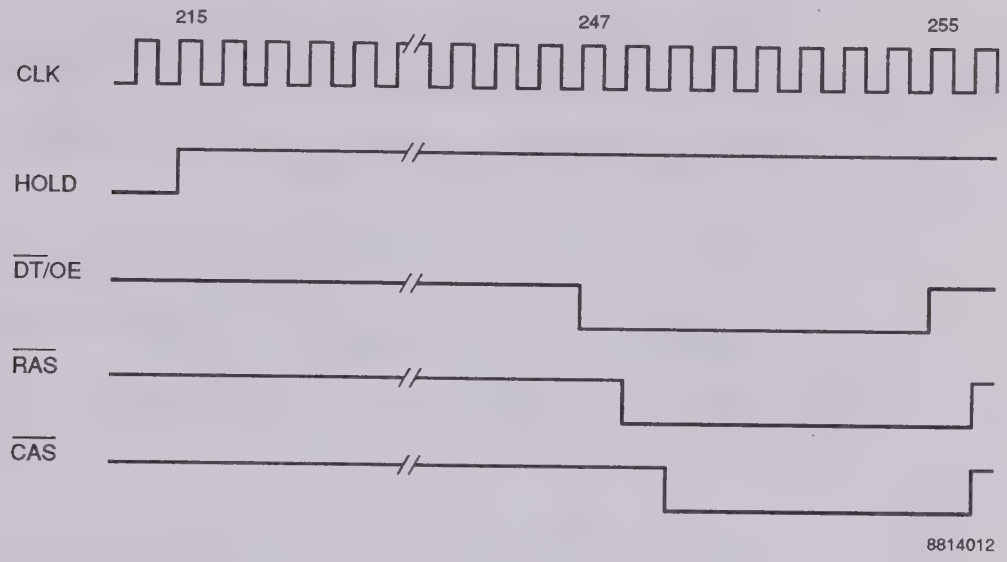
The Pulse Generator section of the Pulse PC Board Assembly consists of XILINX LCA U11011, Video RAMs (U11009, U11010), Buffers (U11012, U11013), Multiplexers (U11006, U11007), Delay Lines (U11008, U11030 through U11032), Jumper Terminal Blocks (JTB11001 through JTB11003) and associated components.

The Video RAMs are dual port with random access available to U12001 on the Processor PC Board Assembly and serial access to U11011. U12001 reads and writes to the Video RAMs in the same manner as with any RAM except access is controlled through U11011. Video RAMs U11009 and U11010 are accessed when $\overline{MCS1}$, ALE and either $\overline{WR}$ or $\overline{RD}$ are activated. Addresses are strobed in using Multiplexers U11006 and U11007. When $\overline{RAS}$ goes low, the select line to U11006 and U11007 stays high because $\overline{RAS}$ used to control the Multiplexers is delayed 10 ns through U11008. This allows A8 through A15 to be latched to the Video RAMs, selecting the row address. After the delay, the Multiplexers with the select line low are set to latch A0 through A8 to the Video RAMs, selecting the column address when $\overline{CAS}$ goes low. $\overline{DT/OE}$ goes low for a read operation or $\overline{RWR}$ goes low for a write operation.

Serial access by U11011 is a read only function. The Video RAMs transfer rows (256 bytes/row) of data into internal Serial Access Registers and sent to U11011 at a rate of one byte each clock count. Serialized data is sent out with each bit line connected to a specific output as follows:

| Video RAM Output | Pin Number | U11011 Output | Pin Number |
|---|---|---|---|
| S0 | U11011-24 | $\overline{Ext\ Pulse}$ | U11011-28 |
| S1 | U11011-29 | $\overline{Ext\ SLS}$ | U11011-30 |
| S2 | U11011-31 | Ext DPSK | U11011-32 |
| S3 | U11011-33 | Scope Trigger | U11011-34 |
| S4 | U11011-36 | Ext Sync | U11011-37 |
| S5 | U11011-40 | BDPSK | U11011-41 |
| S6 | U11011-38 | BPulse | U11011-39 |
| S7 | U11011-42 | PPMG | U11011-43 |

Pulse Generator Serial sequence (Refer to 2-2-1, Figure 12.):




Pulse Generator Data Transfer Timing Chart
Figure 12

- U12001 programs pulses as directed by the Front Panel Processor PC Board Assembly, into the Video RAMs.
- U12001 programs a stop byte (10010000) into an address XXFEh (255th byte) corresponding to the desired row to end on.
- U12001 programs 256 bytes of cleared memory (lows or zeros).
- U12001 programs the starting address using the $\overline{\text{STADD}}$ line for access.
- U11004 BEGIN line to U11011 (U11011-19) goes high to trigger the start of Data Transfers, setting the internal counter to 191h.
- After the 215th byte of cleared memory, HOLD output (U11011-53) goes high to request access to the address lines from U12001.
- HLDA input (U11011-20) goes high informing U11011 that U12001 relinquishes address line control.
- After the 247th byte, $\overline{\text{DT/OE}}$ goes low to set up the Video RAMs for a data transfer to the output registers.
- $\overline{\text{RAS}}$ goes low on the next clock count. Row address determined by the programmed starting address is selected.
- $\overline{\text{CAS}}$ goes low on the following clock count and a zero address from U11012 (enabled by U11011) causes the data transfer to start at address zero in the Serial Access Register.

Pulse Generator Serial sequence (continued):

- After the 255th byte of cleared memory is shifted out of the registers, $\overline{DT/OE}$ goes high, triggered by an internal counter in U11011 that tracks 256 clock counts.
- Data transfer occurs. 256 new bytes from the selected row are loaded into the Video RAM registers.
- Each data transfer is followed by a $\overline{CAS}$ before $\overline{RAS}$ refresh. When no data transfers are occurring, refresh takes place every 12.8 µs.
- With each 50 ns (20 MHz) clock count, one byte (one bit for each output) is shifted out the registers to U11011.

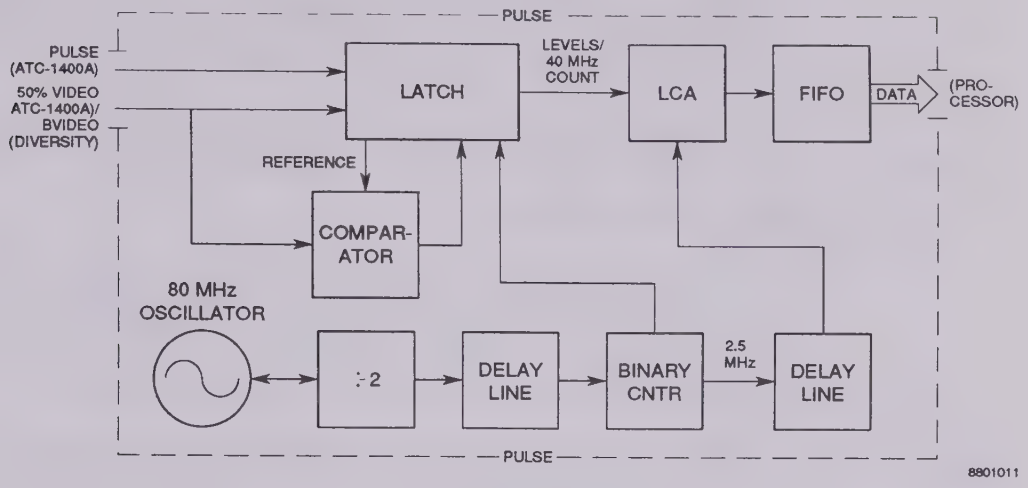
  **NOTE:** The row loaded into the Video RAM registers is being sequentially sent continuously to U11011, regardless of what is selected or transferred.

- Process repeats with data transfers occurring every 12.8 µs. New rows (next row is loaded as incremented by an internal timer in U11011) are transferred and sent out until the programmed stop byte is encountered. The last data transfer takes place followed by the 256 bytes of cleared memory.
- The stop byte also initiates an interrupt (INT1) to U12001.

  **NOTE:** Operation can be manually started or stopped by the Microprocessor U12001 on the Processor PC Board Assembly by using the START or STOP lines.

Buffer/Driver U11013 isolates and boosts signals out of the Test Set. Diodes CR11011 through CR11026, CR11029 through CR11030 and associated components clamp the lines to prevent spikes from ground to +5 V. Transistor Q11003 converts External DPSK TTL to Bipolar output prior to J10015, EXT DPSK. DPSK AMPLITUDE BALANCE Adjust R11026 keeps the individual phase shifts even in amplitude with each other. Jumper Terminal Block JTB11001 sets Delay Line U11030 for correct Antenna A $P_2$ to SPR spacing (2.75 µs [±10 ns]). Jumper Terminal Block JTB11002 sets Delay Line U11031 to align Antenna B $P_1$ pulse position with Antenna A $P_1$ pulse position. Jumper Terminal Block JTB11003 sets Delay Line U11032 as a coarse adjustment for correct Antenna B $P_2$ to SPR spacing.

(b) Edge Detect (Refer to 2-2-1, Figure 13.)




Edge Detect Block Diagram
Figure 13

The Edge Detect circuit consists of XILINX Logic Cell Array (LCA) U11024, Delay Lines U11020 and U11023, Dual J-K Flip-Flop U11018, Comparator U11017, Latch (D Flip-Flop) U11022, Counter U11021, FIFO U11025 and associated components.

The Edge Detect circuit looks for an edge on the two input lines. A comparison circuit compares the level of the incoming data with the last data stored. When it is different, the level of the data and time that the level occurred is stored. One use of the Edge Detect circuit is measuring reply delays. Reply delays are measured by subtracting the time stored of the last lowering edge of the interrogation from the time of the first rising edge of the reply. Because a 40 MHz clock (25 ns/Hz) is used in the counting process, the time is multiplied by 25 ns to obtain the reply delay.

The 40 MHz clock used by the Edge Detect circuit is obtained from an 80 MHz oscillator circuit that is divided in two. Q11002 and associated components make up the 80 MHz oscillator. Q11002 drives the tank circuit C11037 and L11006. Collector impedance is matched down to 50 Ω by L11005 and C11040. The signal drives Crystal Y11001 to the base of Q11002. Phase shift from the base of Q11002 back through the Crystal is 360° with zero dB gain. L11006 is adjusted for maximum amplitude at C11040.

**NOTE**: Because Y11001 is a fifth overtone crystal, L11006 has limited control in pulling circuit to the desired 80 MHz frequency. If L11006 is adjusted more than 10 kHz from maximum amplitude, the risk of the oscillator not starting is greatly increased. If circuit frequency is off to where operation is hindered, Y11001 may be faulty.

The oscillation signal is tapped off the oscillator at C11040 and sent through buffer amplifier Q11001 for isolation. Inverter/Buffers U11019A and U11019B convert the 80 MHz signal to TTL levels that drive J-K Flip-Flop U11018B. U11018B divides the signal in half to the 40 MHz clock with a 50% duty cycle, required by the Edge Detect Circuit.

The 40 MHz clock, used to clock U11018A, also goes through a 10 ns Delay Line U11020 to clock Binary Counter U11021.

Edge Detect sequence:

- Interrogations on the Pulse line are sent to Comparator U11017 (U11017-10) and Latch U11022 (U11022-4). Antenna A replies through the ATC-1400A (50% Video) or Antenna B replies through the S-1403C are sent through OR Gate U11016B to Comparator U11017 (U11017-12) and Latch U11022 (U11022-3).

- U11017 compares last levels (U11017-9 and 11) from Latch U11022 with incoming levels (U11017-10 and 12). When levels are different, A=B output (U11017-6) goes low to J-K Flip-Flop U11018A.

- When clocked, U11018A $\overline{Q}$ output goes high, clocking U11022 and preparing U11024 (U11024-19).

- U11022 latches the new levels back to Comparator U11017, restoring the high on A=B, and to LCA U11024 (ED0-ED1). Four bits (L0-L4) of 40 MHz time, as recorded by Binary Counter U11021, are delayed enough by U11020 to allow the count at the time of the level change to be stored before the count changes.

- This count, along with the levels, are added to a 10-bit count internal to U11024. The internal counter is set up by a 2.5 MHz clock tapped off the Binary Counter U11021 (U11021-11) and delayed 40 ns by U11023 to maintain correct timing.

- When U11018A, $\overline{Q}$ goes high, U11024 sends a low on the write line to FIFO U11025.

- The timing count and signal levels are sent in two successive byte transfers from U11024 to U11025. Refer to 2-2-1, Table 4 for byte formation.

- U11024 sends a reset to U11018A (pin 5).

- FIFO U11025 has DRQ1 go high, requesting DMA on Processor PC Board Assembly. When DMA takes control, data is read (at address $\overline{PCS2}$+2h through U11014 and U11015) at a speed compatible with Processor U12001 on the Processor PC Board Assembly.

- After an interrogation and reply sequence, U12001 on the Processor PC Board Assembly resets U11024 (U11024-12), at address $\overline{PCS2}$+1h through U11014 and U11015.

| BYTE 1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT NUMBER: | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| NAME: | T0 | T1 | T2 | T3 | T4 | T5 | T6 | T7 |
| LINE: | L0 | L1 | L2 | L3 | Internal 10-bit counter | | | |
| FROM: | U11022 | | | | U11024 | | | |
| BYTE 2 | | | | | | | | |
| BIT NUMBER: | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| NAME: | T8 | T9 | T10 | T11 | T12 | T13 | Interr Pulse | Reply Pulse |
| LINE: | Internal 10-bit counter | | | | | | ED1 | ED0 |
| FROM: | U11024 | | | | | | U11022 | |

Edge Detect Byte Formation
Table 4

(c) Reply Decoder

The Reply Decoder is designed to decode the pulse position modulation (PPM) data in Mode S replies. The Reply Decoder circuit consists of XILINX LCA U11027 and Binary Counter U11026. U11027 decodes the Mode S replies while the Binary Counter U11026 provides an 8 MHz clock used internally by U11027.

U11027 is selected by U12001 on the Processor PC Board Assembly at the following addresses:

$\overline{PCS2}$+60h to read the decoded reply data,
$\overline{PCS2}$+63h to clear the count,
$\overline{PCS2}$+64h to count the number of ATCRBS replies through Antenna A,
$\overline{PCS2}$+65h to count the number of ATCRBS replies through Antenna B,
$\overline{PCS2}$+66h to count the number of Mode S replies through Antenna A,
$\overline{PCS2}$+67h to count the number of Mode S replies through Antenna B,
$\overline{PCS2}$+68h to read the Test Byte,
$\overline{PCS2}$+69h to write the Test Byte.

These are selected through Decoder U11014 when $\overline{BPCS2}$ ($\overline{PCS2}$), U11014-5 is low and Address Latch Enable (ALE [U11014-4]) is low. A5 (U11014-2) and A6 (U11014-3) are high (60h) while the state of A0 through A3 bits to U11027 dictate the rest of the address.

The Test Byte allows Processor U12001 on the Processor PC Board Assembly to determine if the new Pulse PC Board Assembly is installed (for an S-1403 converted to an S-1403C).

U11027 is triggered off the 8 µs long Mode S reply preamble. If triggered by a squitter, U11027 sends an interrupt on PA2 to the Serial/Parallel I/O U12005 on the Processor PC Board Assembly. PPM Data is received by U11027 at pin 21, BVIDEO (from the Diversity Module) and pin 20, 50% VIDEO (from the ATC-1400A).

U11027 begins decoding data as it is received. When U11027 receives eight bits, DRQ0 goes high requesting DMA action from the Processor U12001 on the Processor PC Board Assembly. All replies are written to the internal FIFO (U11027). When a Mode S reply is received, the first byte written to the FIFO is a status byte. When data is read, DRQ0 is reset back to low. This occurs eight times (status byte and 56-bit short message) or 15 times (status byte and 112-bit long message) until the entire reply with status byte is received, decoded and read.

U11026 provides the 8 MHz clock by taking the 40 MHz signal from U11018B and dividing it by five. Qc output (U11026-12) goes high every fifth count and is fed into U11027. The high is also inverted by U11019C and a low input on Load (U11026-9) causes the counter to reset to zero.

(d) Control

The Control section has several functions in addition to the process of selecting other circuits on the Pulse PC Board Assembly. One main function is the programming of the four XILINX LCA components on the Pulse PC Board Assembly. The Control section selects the clock source, sync source, sync delay and Pulse Power Measurement Gate (PPMG) fixed position. Two discrete pulses are also generated by the Control section. Most functions are carried out by XILINX LCA U11004. In addition to U11004, the circuit contains Decoders U11014 and U11015, Latch U11002, Multiplexer U11003 and EPROM U11005.

The LCA XILINX components lose their programming when power is turned off. When power is applied to the S-1403C, EPROM U11005 reprograms the XILINX components starting with U11004. When U11004 is full, programming continues out of U11004 (U11004-59) to U11011 (U11011-58). When U11011 is full, programming continues out of U11011 to U11024 and finally to U11027. Other signals used in the power up process are CCLK, used to clock in the data, and D/$\overline{P}$ which goes high when programming is complete on all XILINX parts. LCA XILINX components also reprogram when instructed by U12001 on the Processor PC Board Assembly. Reset goes low and is inverted high through U11038C to activate transistors Q11005 and Q11004. The circuit consisting of Q11004, U11036A and U11036B cause U11027, U11024, U11011 and U11004 to reprogram on $\overline{\text{RES XILINX}}$ line. Q11005 causes NAND Gate U11035A to go high to deactivate Buffer U11034, keeping INT1 (BINT1) and HOLD (BHOLD) lines to the Processor PC Board Assembly from changing states while the XILINX parts are reprogramming.

U11004 is selected with addresses $\overline{\text{PCS2}}$+50h for sync delay and $\overline{\text{PCS2}}$+51h for the control byte. Selection is accomplished through Decoders U11014 and U11015 (ALE, $\overline{\text{BPCS2}}$, A5 and A0 low with A6 and A4 high for $\overline{\text{PCS2}}$+50h; ALE, $\overline{\text{BPCS2}}$ and A5 low with A0, A6 and A4 high for $\overline{\text{PCS2}}$+51h).

Sync delay sets the delay between the sync source selected and when U11024 initiates an output on the BEGIN line to the Pulse Generator and Edge Detect Sections. Sync delay is programmed on the data bus with a number from zero to 253. Actual delay is calculated using the following formula: (254 - programmed number) + 0.1 µs = sync delay.

The control byte uses three bits to control PPMG output, pre-pulse and ATCRBS/Mode S pulse. Bit D0, setting PPMG output, is low (no delay) when measuring ATCRBS replies and high (125.1 µs delay) to save Video RAM room when measuring Mode S replies. Bit D1 controls pre-pulse operation with low deactivating pre-pulse and high activating pre-pulse. Bit D2 controls ATCRBS/Mode S pulse operation with low deactivating ATCRBS/Mode S pulse and high activating ATCRBS/Mode S pulse.

Another control byte is selected through Octal D Flip-Flop, Latch U11002 at address $\overline{PCS2}$+40h. Bit D0 is not used at this time. Bit D1 controls the Pulse Generator Output Enable line. Pulse outputs are enabled when D1 is low and tri-stated when D1 is high. Bit D2 selects the Hold Enable line. Bits D3 and D4 select the clock source. When both bits are low, the external clock test point (TP11001) to load an external clock is selected. When D3 is high with D4 low, the 20 MHz clock from the ATC-1400A is selected (usual mode of operation). When D3 is low with D4 high, no clock is selected. When both D3 and D4 are high, the 20 MHz clock tapped off of U11021 is selected. Bit D5 controls the Ext Mod input, through Line Receiver U11001. When D5 is low, Ext Mod is deactivated through U11001. When D5 is high, the signal on Ext Mod is converted to TTL by U11001 and applied to the signal that is eventually sent out the ATC-1400A RF I/O Connector. U11001 also converts the Ext Sync, if used, to TTL. Bits D6 and D7 select the sync source through U11004 (U11004-20 and 21). When D6 and D7 are low, the Self Interr from the ATC-1400A is selected as the sync source (usual mode of operation). When D6 is high with D7 low, a 50 ns pulse is sent out on the BEGIN line with no delay (used in BURST functions). When D6 is low with D7 high, no sync source is selected. When both D6 and D7 are high, the Ext Sync input becomes the sync source.

(e) RF Vernier

The RF Vernier section, consisting of Digital to Analog Converter (DAC) U11029, provides an analog voltage used to control RF gain in addition to the ATC-1400A RF level. An adjustment range of ±3.0 dB is accomplished through the RF Vernier section.

RF Vernier sequence:

- U11029 is selected to be written to by U12001 on the Processor PC Board Assembly.
- Address $\overline{PCS2}$+5h (ADL goes low) is selected through U11014 and U11015, preparing U11029 to receive the first bits of RF level information.
- Data Bits DB0 through DB7 are loaded via D0-D7 into U11029.

RF Vernier sequence (continued):

- Address $\overline{PCS2}$+6h (ADH goes low) is selected through U11014 and U11015, preparing U11029 to receive the last two bits of RF level information.

- Data Bits DB8 through DB9 are loaded via D0-D1 into U11029 making a total of 10 information bits.

- U11029 converts the input data to an output voltage that is sent through J10013 to the ATC-1400A, J4. When DB0 through DB9 are low, the voltage output at U11029 is 0 Vdc. When DB0 through DB9 are high, the voltage output at pin 20 is 7.0 Vdc nominally. Various data inputs in between provide voltages corresponding to 0.1 dB increments.

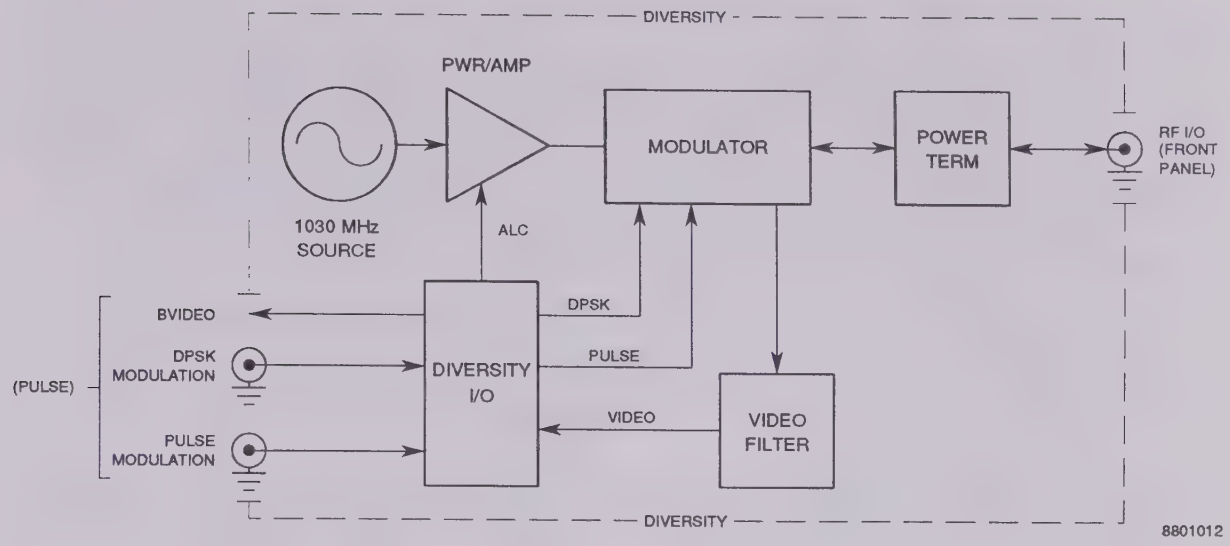
Amplifier U11028A and resistors R11019, R11020, R11021 and R11030 provide a voltage reference circuit. FULL SCALE Adjust R11021 sets the full scale voltage (+7.0 Vdc nominal value) and ZERO SCALE Adjust R11023 sets a zero gain voltage (+1.3 Vdc nominal value) to counteract error current.

(5) Diversity Module (Refer to 2-2-1, Figure 14 [w/o MLD] or Figure 15 [w/ MLD].)

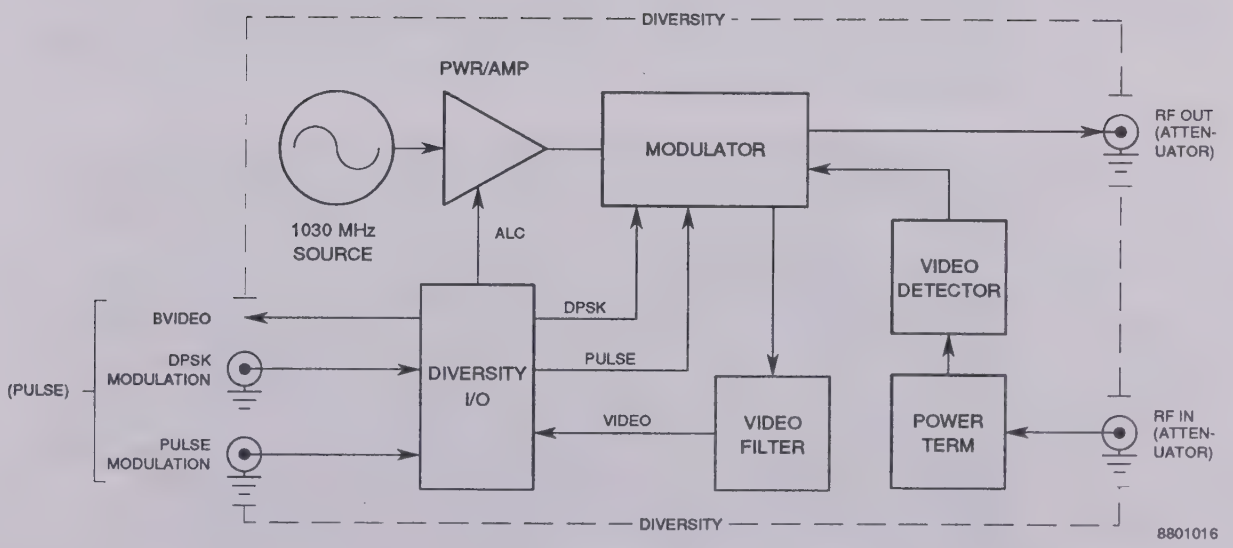
The Diversity Module consists of:

10 MHz TCXO
1030 MHz Source PC Board Assembly
Power Amp PC Board Assembly
Diversity I/O PC Board Assembly
Modulator PC Board Assembly
Power Termination Assembly
Video Filter PC Board Assembly
Video Detector PC Board Assembly (only with MLD)

The Diversity Module functions as a second L-Band transmitter (first being the ATC-1400A) and is used for testing Mode S Transponders with diversity (two distinct antenna connectors). The primary transponder antenna (Antenna A ) is connected to the ATC-1400A RF I/O Connector. When applicable, the secondary transponder antenna (Antenna B) is connected to the S-1403C ANT B Connector. The Diversity Module generates Differential Phase Shift Keying (DPSK) and Pulse modulated interrogations for Mode S Transponders. The Diversity Module detects pulse modulated signals from transponders.




Diversity Module w/o MLD Block Diagram
Figure 14

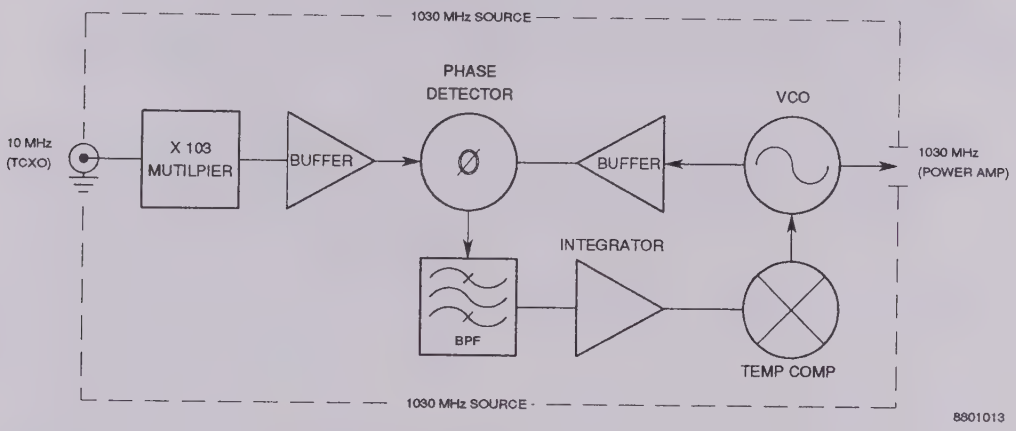



Diversity Module w/ MLD Block Diagram
Figure 15

(a) 10 MHz TCXO

The 10 MHz Temperature Compensated Crystal Oscillator (TCXO) U23001 provides the 10 MHz input to the 1030 MHz Source PC Board Assembly. The Power Distribution PC Board applies power (6 Vdc) to the TCXO at J23017. The TCXO has 2 parts per million accuracy to achieve frequency specifications. The 10 MHz, at >1 Vrms, is sent through J23008 to the 1030 MHz PC Board Assembly. A course adjustment is provided to maintain frequency as the crystal ages.

(b) 1030 MHz Source PC Board Assembly (Refer to 2-2-1, Figure 16.)




1030 MHz Source PC Board Assembly Block Diagram
Figure 16

The 1030 MHz Source PC Board Assembly, part of the Source/Pwr Amp Assembly, uses a Voltage Controlled Oscillator (VCO) to provide the 1030 MHz signal. The frequency is kept tuned by a Multiplier using the TCXO reference, Phase Detector, Error Amplifier (Integrator) and Temperature Compensator.

The frequency reference from the TCXO enters the 1030 MHz Source PC Board Assembly at J30009 into the Multiplier. The 10 MHz signal drives the base of high current amplifier Q24002, biased by current controller Q24001, using a regulated +11 V from the Diversity I/O PC Board Assembly. Q24002 drives high level current to snap diode CR24002 (Multiplying Varactor). Voltage across R24049 sets the reference for CR24002. L24002 and C24004 provide matching impedance to increase the multiplying efficiency of CR24002. 10 MHz spectral lines are generated by CR24002. C24005 and printed transmission line L24011 form a Tank Circuit tuned to 1030 MHz, bringing up the 103rd harmonic. The signal, monitored through TP23002, feeds a three-stage linear Buffer amplifier consisting of saturable transistors Q24003, Q24004 and Q24005. The Buffer, tuned to 1030 MHz, increases the power of the desired harmonic (1030 MHz) to drive an input to the Phase Detector HY24001.

The Voltage Controlled Oscillator (VCO) provides the other input. A regulated +11 V from the Diversity I/O PC Board Assembly supplies power to the oscillating transistor Q24006. Transmission line-capacitor circuits L24007-C24027, L24028-C24028 and L24029-C24029 cause Q24006 output to match the frequency determining element, Resonator HY24002. Temperature compensator C24047 and Varactor CR24004 keep the oscillator tuned to 1030 MHz. Power is coupled off the oscillator through HY24002 and is fed through a Buffer amplifier, composed of saturable transistors Q24007, Q24008 and Q24009. The Buffer, also tuned to 1030 MHz, provides a level to drive the local oscillator input to HY24001.

HY24001 and CR24003 comprise a Phase Detector providing a dc error voltage proportional to the phase difference detected between the VCO local oscillator and Multiplier inputs. This voltage is filtered by Bandpass Filter C24021, L24006 and C24022 and sent to Integrator U24001.

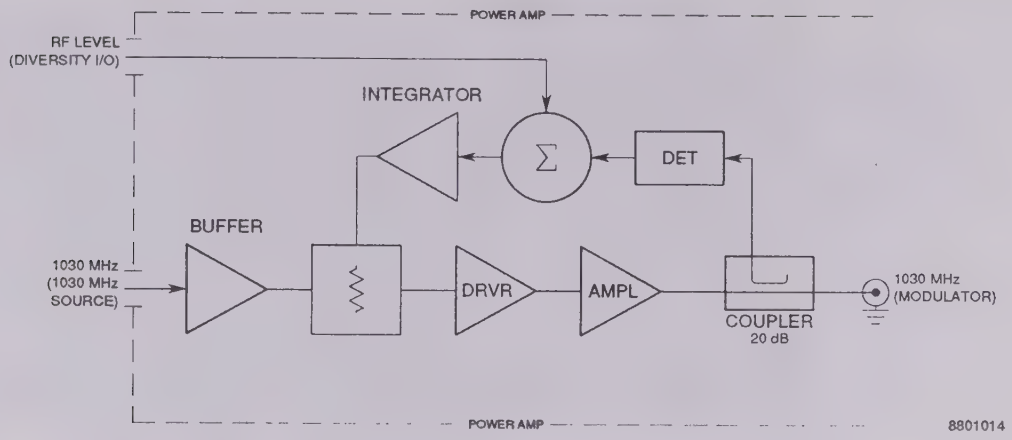
When the VCO output frequency equals the Multiplier (Reference) output frequency, Phase Detector voltage output to U24001 is minimal, causing negative feedback. U24001 and associated circuitry act as a phase-locked loop filter. When the VCO and Multiplier frequencies become different, pin 3 on U24001 becomes more positive. As the frequency difference increases, U24001 becomes a Wien Bridge Oscillator. The ac output feeds the VCO tuning Varactor CR24004, adjusting the resonating frequency, fed to HY24001, until the error voltage is reduced to where U24001, again, acts as a phase-locked loop filter. OFFSET R24022 sets a voltage level to compensate for imbalances in the Phase Detector and/or Buffers. DEVIATION R24025 sets the ac deviation voltage limit to prevent the VCO from setting on the 102nd or 104th harmonics.

Q24010 and Q24011 provide temperature compensation. While Q24010 exponentially increases current with temperature, Q24011 is the high impedance load providing temperature compensated voltage to VCO Varactor CR24004. VCO Tune Voltage, nominally 4 Vdc, may be checked at TP23007 and is set by R24026.

(c) Power Amp PC Board Assembly (Refer to 2-2-1, Figure 17.)

The Power Amp PC Board Assembly, on the Source/Pwr Amp Assembly, provides signal amplification to +20 dBm. The Power Amp uses an Automatic Level Control (ALC) circuit to achieve amplitude consistency.

The 1030 MHz signal from the 1030 MHz Source PC Board Assembly is fed into the Power Amp PC Board Assembly to the base of Q27001. Q27001 and Q27002 form a two-stage Buffer, primarily to provide reverse isolation from the Power Amp to the VCO. The isolated 1030 MHz signal may be seen at TP23001 before it goes to Pin Attenuator Diodes CR27003 and CR27004. The attenuation provided by CR27003 and CR27004 and adjusted by the ALC circuit sets the input signal level to the Power Amp Driver Q27004. Q27004 steps up the signal to drive the Power Amp Q27006. Q27005 and associated circuitry provide current control to Q27006. Printed transmission lines C27029, L27010, L27011, L27012, C27030, L27013, L27014, L27015 and C27031 provide matching impedance while C27032, L27016, C27033, L27017 and C27034 filter out unwanted harmonics. The 1030 MHz signal at a nominal +15 dBm is sent off the Power Amp PC Board Assembly through J30010.

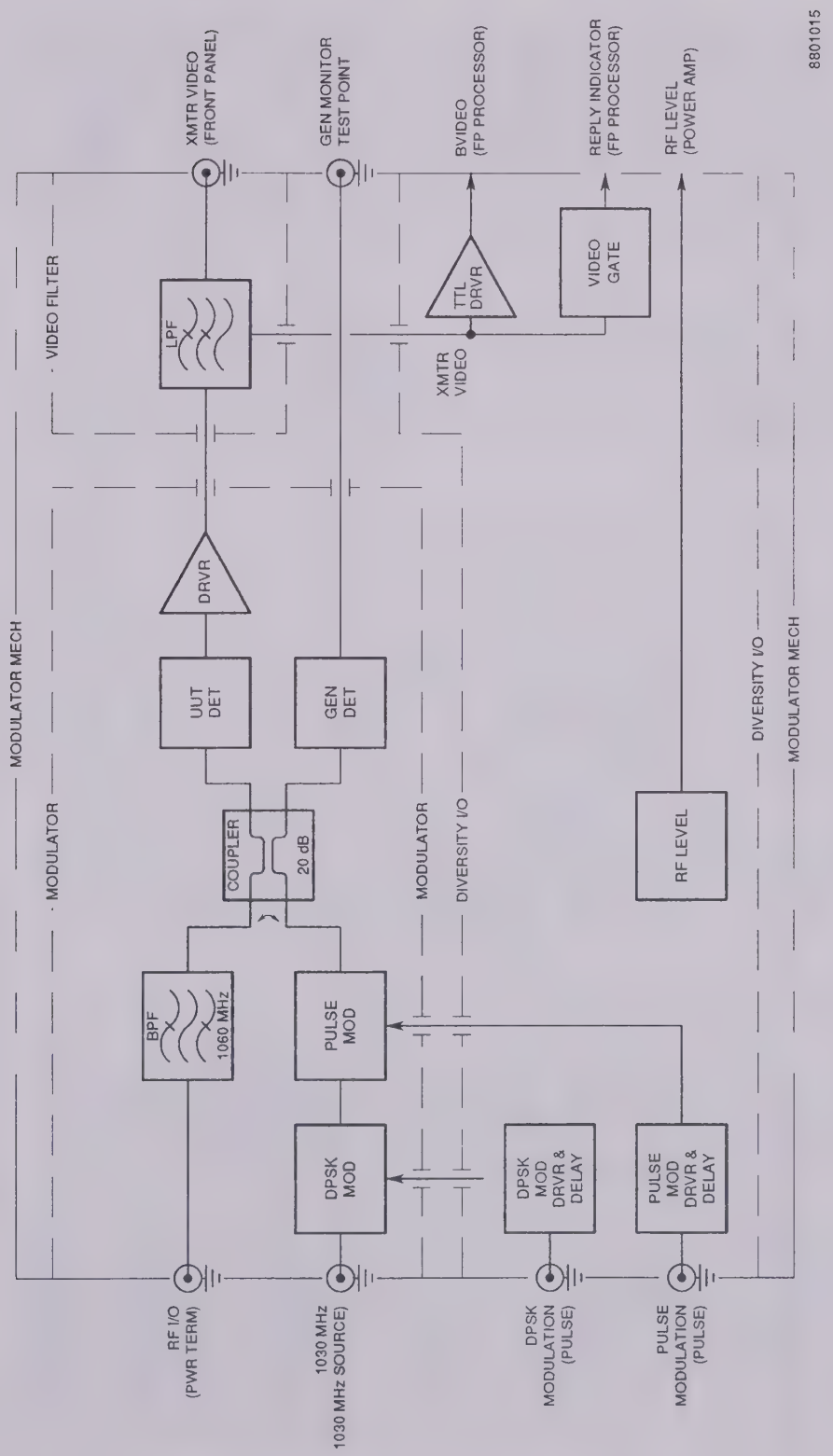



Power Amp PC Board Assembly Block Diagram
Figure 17

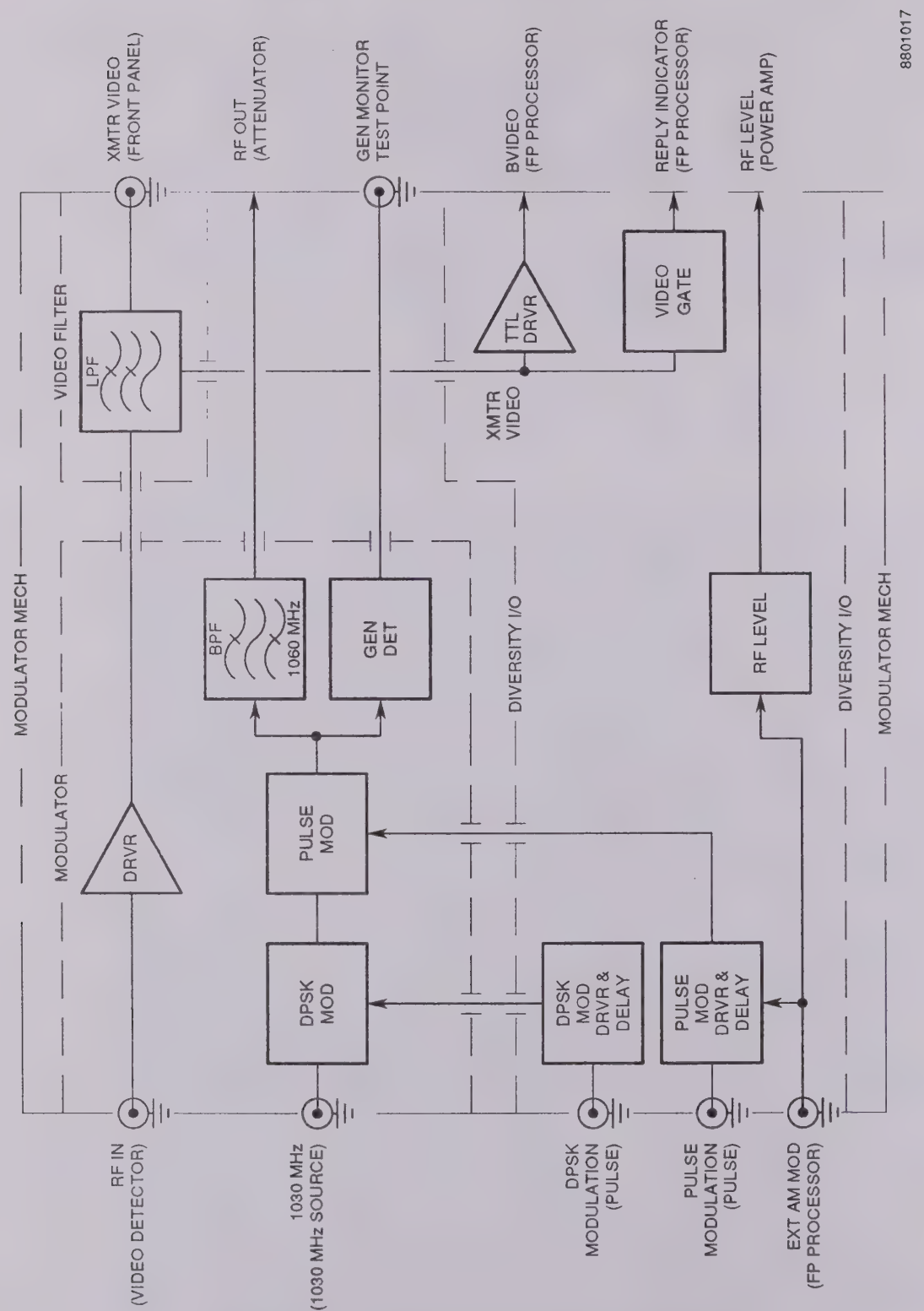
Automatic Level Control (ALC) is accomplished as Directional Coupler HY27001 couples the RF of the 1030 MHz Connector J30010 to Detector CR27006, reducing the signal by 20 dB to a nominal -5 dBm. CR27006 provides a dc level proportionate to the output level of the Power Amp. The resulting dc voltage across R27017 and R27019 is summed together with the voltage derived from an RF reference level and is applied to the negative input (U27001-2) to Error Amplifier U27001. The RF reference level from the Diversity I/O PC Board Assembly, is applied to CR27007. CR27007 provides temperature compenstation of the RF reference level. The dc reference voltage across R27020 (read from test points TP27001 and TP27002) is set by BIAS ADJ R27021 to be equal to the Power Amp Detector bias voltage across R27017 (read from test points TP27004 and TP27005). U27001 amplifies and inverts the summed error signal. The error voltage output from U27001 may be monitored at ALC Voltage test point TP27003. Q27003 provides a current source, proportional to the error voltage, that controls Pin Attenuator Diodes CR27003 and CR27004. When Power Amp level goes low, CR27006 current goes low and U27001-2 input is low causing U27001-6 output to go high. Current from Q27003 increases through CR27003 and CR27004 reducing their effective resistance, increasing the signal level input to Driver Q27004. Power Amp output increases accordingly. When Power Amp level goes high, CR27006 current goes high and U27001-2 input is high causing U27001-6 output to go low. Current from Q27003 decreases through CR27003 and CR27004 increasing the effective resistance, dropping the signal level input to Q27004. Power Amp output decreases accordingly.

(d) Diversity I/O PC Board Assembly (Refer to 2-2-1, Figure 18 [w/o MLD] or Figure 19 [w/ MLD].)

The Diversity I/O PC Board Assembly, on the Modulator Assembly, provides Modulation Drivers for the DPSK and Pulse signals, the regulated +11 Vdc for the 1030 MHz Source PC Board Assembly and the RF reference level for the Power Amp PC Board Assembly. The Diversity I/O PC Board Assembly also converts XMTR VIDEO to a usable TTL signal for the Front Panel Processor PC Board Assembly.




Modulator Assembly w/o MLD Block Diagram
Figure 18




Modulator Assembly w/ MLD Block Diagram
Figure 19

The DPSK Modulation circuit, controlled by the TTL signal from the Pulse PC Board Assembly, quickly turns on and off the Modulator PC Board Assembly Pin Diodes CR25013 and CR25014. R26003, R26005, C26004 and U26002C provide a falling edge position adjustment for the DPSK modulation signal. R26006, C26005 and U26002D provide a rising edge position adjustment. R26030 provides the steady state on current for the Modulator PC Board Assembly Pin Diodes CR25013 and CR25014. R26029, R26028, Q26006, R26041 and R26027 provide the steady state off voltage for CR25013 and CR25014. C26016, CR26002 and Q26003 provide a current spike on the rising edge of the DPSK modulation signal. C26017, CR26003 and Q26004 provide the current spike on the falling edge. The current spikes turn CR25013 and CR25014 on very quickly, providing a clean phase transition. DPSK OFF VOLTAGE ADJ R26027 sets the steady state off voltage for approximately -3 Vdc. FALLING EDGE COMPENSATION R26028 adjusts the amplitude balance of the DPSK modulated signal. Variable Resistors R26006 and R26005 adjust DPSK Modulation position.

R26007, R26009, C26007 and U26002B provide an adjustable falling edge delay for the pulse modulation signal. R26010, C26008 and U26002A provide an adjustable delay for the leading edge of the pulse modulation signal. Transistors Q26010 and Q26011 form a differential amplifier, providing the on current for the pulse modulation Diodes CR25006, CR25007 and CR25008 on the Modulator PC Board Assembly and reverse biasing of CR25005. Transistors Q26012 and Q26013 form a differential amplifier, providing the current for activating CR25005 on the Modulator PC Board Assembly and reverse biasing of CR25006 CR25007 and CR25008. Q26014 servos the rise and fall current with power level to keep the rise and fall times stable over the range of the Antenna B RF Vernier (with MLD) or provides a fixed value of off current (without MLD). R26054 and RISE TIME adjustment R26055, set the on current, controlling the rise time. FALL TIME adjustment R26058, R26059 and R26060 set the off current, controlling the fall time. Variable Resistors R26010 and R26009 adjust Pulse Modulation position.

XMTR VIDEO, (0.5 V nominal) from the Video Filter PC Board Assembly, is converted to TTL level by Q26001, Q26002 and associated circuitry. BIAS ADJ R26017 maintains the sensitivity level, setting the biasing to turn on and off Q26001 and Q26002. The TTL signal goes through the One-Shot Driver Q26009, turning on Monostable Multivibrator U26004A. U26004A operates as a 0.5 second one shot to illuminate Front Panel UUT XMTR Indicator DS15002. The BVideo TTL signal is also sent to the Pulse PC Board Assembly, driven by Inverter Buffer/Driver U26003A.

U26001 provides the regulated +11 Vdc for the 1030 MHz Source PC Board Assembly. R26001 and R26002 set the regulation level while C26002 and C26003 stabilize the circuit from glitches. The primary purpose for this circuit is to provide an on/off control to effectively shut down the VCO signal and Multiplier output when the Diversity Module is switched off by the Front Panel Processor PC Board Assembly. The +11 V Regulator provides a clean, regulated +11 V that reduces the phase noise of the VCO and Multiplier.

The RF Reference circuit consists of a voltage divider network (R26024, CR26001 and R26013) and Buffer/Driver U26005. CR26001 stabilizes the voltage drop while RF LEVEL ADJ R26013 adjusts the output of U23005 to the nominal -0.2 V used by the Power Amp PC Board Assembly. With MLD, the EXT AM MOD input (J23001-5) from the Front Panel Processor PC Board Assembly servos the Antenna B RF vernier reference voltage to U26005A. U26005A provides the Antenna B RF reference level to the ALC circuit on the Power Amp PC Board Assembly to provide the Antenna B ±3.0 dB vernier (with MLD).

U26005B and associated components provide a level shift and offset to the RF Level to provide a bias voltage for CR25005 on the Modulator PC Board Assembly. With MLD, the circuit controls the position of the rising edge of the RF pulse to maintain constant position over the ±3.0 dB Antenna B vernier range. Without MLD, the circuit is set for 0 V. BIAS GAIN R26068 sets the level shift. BIAS OFFSET R26064 sets the reference or offset.

(e) Modulator PC Board Assembly (Refer to 2-2-1, Figure 18 [w/o MLD] or Figure 19 [w/ MLD].)

The Modulator PC Board Assembly, part of the Modulator Assembly, applies DPSK and Pulse Modulation to the 1030 MHz source signal when transmitting and provides UUT signal detection when receiving.

The 1030 MHz, +15 dBm nominal signal received from the Power Amp PC Board Assembly is fed through a Quadrature Hybrid HY25001 for DPSK Modulation. A resistive pad made up of R25057, R25058 and R25059 provides isolation and impedance matching.

DPSK Modulation from the Diversity I/O PC Board Assembly controls the Pin Diodes CR25013 and CR25014. The Pin Diodes, when shut off, act as an open causing the circuit to reflect back the 1030 MHz signal in phase. The Pin Diodes, when turned on, act as a short changing the load impedance so the 1030 MHz signal is reflected back 180° out of phase. Both reflective input circuits to HY25001 are tuned and set to be identical.

**NOTE**: Z25017, Z25019, Z25021 and Z25023 are printed transmission lines that are set one time at the factory.

The 1030 MHz signal from HY25001 goes through a High Pass Filter consisting of C25006, Z25002 and C25005 before being Pulse Modulated. Pin Diodes CR25005, CR25006, CR25007 and CR25008; along with associated components make up the Pulse Modulator. A +3 V potential applied by the pulse modulation causes current to flow freely. CR25006, CR25007 and CR25008 offer little resistance, allowing the 1030 MHz signal to pass through. When turned off by a -3 V potential; CR25006, CR25007 and CR25008 have very high resistance while CR25005 turns on to shunt the signal to ground. The circuit provides 80 dB of isolation between on and off Pulse Modulation.

For transmission (without MLD), the modulated signal at HY25002 is coupled off 20 dB down. With or without MLD, the signal goes through a Bandpass Filter (Capacitors C25007 through C25012 and transmission lines Z25006 through Z25012), wide enough to pass both 1030 MHz and 1090 MHz frequencies. R25048, R25049, R25050 and AT31001 make up an attenuator, reducing the signal another 20 dB (16 dB with MLD) before sending it to the Power Termination Assembly at a nominal -30 dBm through J31012 (without MLD) or the Attenuator Assembly at a nominal -14 dBm through J23018 (with MLD).

Without MLD, the Modulator PC Board Assembly receives the UUT Antenna B transmission through J31012. The UUT signal, also reduced 20 dB by the impedance matching network, passes through the Bandpass Filter, Directional Coupler HY25002 and Resistive Pad (R25012, R25013, R25014 and R25015). Signal modulation is detected by CR25009 and Z25015. The UUT signal is then coupled to the Video Line Driver circuit across C25013. UUT signal is buffered by Q25004 and Q25005 to drive a 50 Ω load.

With MLD, the Modulator PC Board Assembly receives Antenna B Reply Video from the Video Detector through J23019. The signal, coupled to the Video Line Driver circuit across C25017, is buffered by Q25004 and Q25005.

The conditioned Video taken off the Voltage Divider Network R25030 and R25032 is sent to the Video Filter PC Board Assembly. Operational Amplifier U25001 keeps the UUT signal referenced to zero volts. The voltage drop across R25030 is felt at the input of U25001 and the resulting output voltage determines bias for Q25004 and Q25005. CR25012 provides temperature compensation.

Without MLD, TEST VIDEO INPUT TP23004 provides an external source location for evaluating the Video Line Driver circuit on the Modulator PC Board Assembly.

(f) Power Termination Assembly

The Power Termination Assembly provides a 50 Ω termination for the UUT and protects the S-1403C against excessive incoming power through the ANT B Connector (J10002). The Power Termination Assembly is in the transmit and receive circuit between the Modulator Assembly and the UUT when the MLD option is not installed. When the MLD option is installed the Power Termination Assembly is only in the receive circuit between the Attenuator Assembly and the Video Detector PC Board Assembly.

When transmitting (without MLD), the modulated -30 dBm signal from the Modulator PC Board Assembly enters the Power Termination Assembly through RF I/O Connector J28029. Directional Coupler HY28001 reduces the signal another 20 dB. The Antenna B interrogation signal is sent to the UUT through the RF I/O Connector J23014 and ANT B Connector J10002.

The UUT transmits a return reply signal of 1090 MHz with peak pulse power of up to approximately +57 dBm and average power of ≤+40 dBm. The Power Termination Assembly receives the Antenna B return reply signal through RF I/O Connector J23014 from the ANT B Connector J10002 (without MLD) or the Attenuator Assembly (with MLD). The input power is terminated by R28002. The signal decreases 20 dB across Directional Coupler HY28001 before going through RF I/O Connector J28029 to the Modulator Assembly. R28001 with C28001 and L28001 keep the circuit frequency balanced for 50 Ω impedance.

(g) Video Filter PC Board Assembly

The Video Filter PC Board Assembly is a passive 50 Ω, 5 element, Low-Pass filter consisting of C29001, C29002, C29003, L29001 and L29002. The Video Filter PC Board Assembly, part of the Modulator Assembly, provides RF filtering.

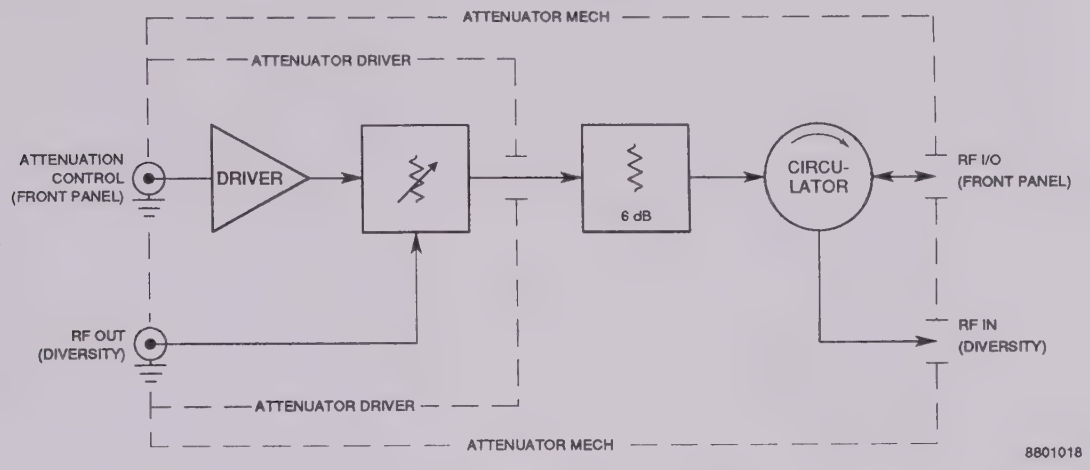
Signals to XMTR VIDEO Connector J23016 provide a 50 Ω Video Connector for the Front Panel. The buffered signal through connector J31015 is sent to the Diversity I/O PC Board Assembly to make BVideo and cause the UUT XMTR Indicator on the Front Panel Assembly to illuminate.

(h) Video Detector (Only with MLD)

The Video Detector PC Board Assembly provides the Reply Video from the UUT transmission for the Modulator PC Board Assembly.

The Video Detector PC Board Assembly receives the UUT signal from the Power Termination Assembly through J13001. Resistive power divider (R13001 through R13005) sets the level for Detector CR13001. CR13001, a Schottky Barrier Diode, linearly detects the signal. Printed element C13003, provides for fast detection. The detected Reply Video signal is sent to the Modulator PC Board Assembly through J13002.

(6) Attenuator Assembly (Only with MLD) (Refer to 2-2-1, Figure 20.)




Attenuator Assembly Block Diagram
Figure 20

The Attenuator Assembly consists of:

Attenuator Driver PC Board Assembly
Line Attenuator
Circulator

The Attenuator PC Board Assembly applies the control signals from the Front Panel Processor PC Board Assembly to the Step Attenuator AT21001. A high input from the Front Panel Processor PC Board on any of the control lines through J21005 activates associated transistor pairs. Increased current flow through the associated diodes set the Attenuator AT21001 for the desired attenuation. The Antenna B transmit signal from the Modulator Assembly enters Step Attenuator AT21001 through J21003 (RF OUT). The attenuated signal is sent to the Line Attenuator AT21002.

Line Attenuator AT21002 decreases the Antenna B transmit signal by approximately 6 dB.

All Antenna B signals go through Circulator HY21001. The transmitted Antenna B signal from AT21002 is sent to the ANT B Connector through J21001 and the Front Panel. The Antenna B signal received from the UUT is sent to the Power Termination Assembly through J21002 (RF IN).

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## 2. Calibration/Verification

### A. General

CALIBRATION/VERIFICATION PROCEDURE — PAGE

Power Supply . . . . . 5
Interrogation Pulses and SPR . . . . . 7
Suppressor and Interference Pulses . . . . . 13
RF Level . . . . . 16
Antenna B . . . . . 18
Reply Delay and PPMG . . . . . 22

(1) Calibration/Verification Schedule

The Calibration/Verification Procedures should be performed as a result of one or more of the following conditions:

- Failure to Meet Specifications

  If, during the course of normal operation, the Mode S Test System or any major function thereof fails to meet the performance specifications in 1-3-1 of the S-1403C Operation Manual, the Calibration/Verification Procedures should be performed.

- Module/Assembly Replacement

  If any one or more of the Mode S Test System modules/assemblies are replaced, the Calibration/Verification Procedures should be performed.

- Annual Calibration/Verification

  IFR Systems recommends an annual Calibration/Verification on the Mode S Test System to maintain proper testing standards.

(2) Controls, Connectors and Indicators

Refer to 2-2-2, Figure 21 for S-1403C controls, connectors and indicators (alphabetic character identifiers). Refer to 2-2-2, Figure 22 for ATC-1400A controls, connectors and indicators (numeric character identifiers).

(3) Disassembly Requirements

Remove top cover from S-1403C according to 2-3-1C(1). Remove top cover from ATC-1400A according to 2-3-1D in ATC-1400A Maintenance Manual.

### B. Performance Requirements

It is strongly recommended that personnel thoroughly read and understand all steps of the procedures to be performed and be familiar with the circuit under test. Knowledge of power, frequency and waveform to be expected at each test point is recommended.

The Mode S Test System must be installed (with calibrated ATC-1400A) according to 1-2-1D in the Mode S Test System Operation Manual.

C. Test Equipment Requirements

Appendix C contains a comprehensive list of test equipment suitable for performing any procedure contained in this manual. Other equipment meeting specifications listed in Appendix C may be substituted in place of recommended models.

**NOTE:** For certain procedures in this manual, the test equipment listed in Appendix C may exceed the minimum required specifications.

D. Preliminary Operations

(1) Safety Precautions

**WARNING: REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY CALIBRATION/VERIFICATION PROCEDURE INVOLVING LIVE CIRCUITS.**

**WARNING: WHEN WORKING WITH LIVE CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET OR BEHIND BACK TO AVOID SERIOUS SHOCK HAZARD.**

**WARNING: USE ONLY INSULATED TROUBLESHOOTING TOOLS WHEN WORKING WITH LIVE CIRCUITS.**

**WARNING: FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AS WELL AS A RUBBER MAT UNDERNEATH TECHNICIAN'S CHAIR.**

**WARNING: HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.**

**CAUTION:** THE MODE S TEST SYSTEM CONTAINS PARTS SENSITIVE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD). ALL PERSONNEL PERFORMING CALIBRATION/VERIFICATION SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES AND/OR BE ESD CERTIFIED.

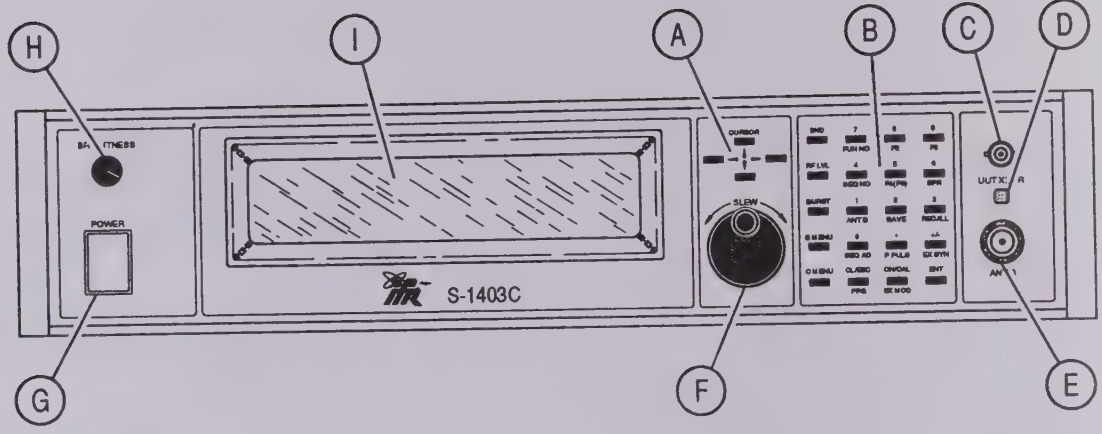
(2) Environmental Considerations

For best results, the calibration environmental conditions should be identical to the environmental conditions at the normal operating location.

E. Test Record

A Calibration/Verification Data Sheet is provided for recording the results obtained while performing the Calibration/Verification Procedures.

**NOTE:** It is recommended the technician reproduce copies of the Calibration/Verification Data Sheet, rather than use the copy in this manual.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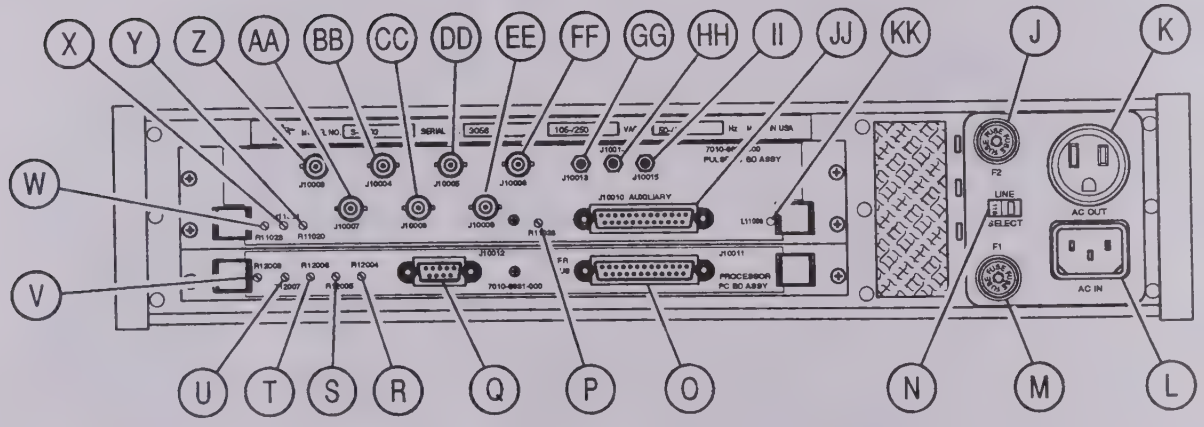
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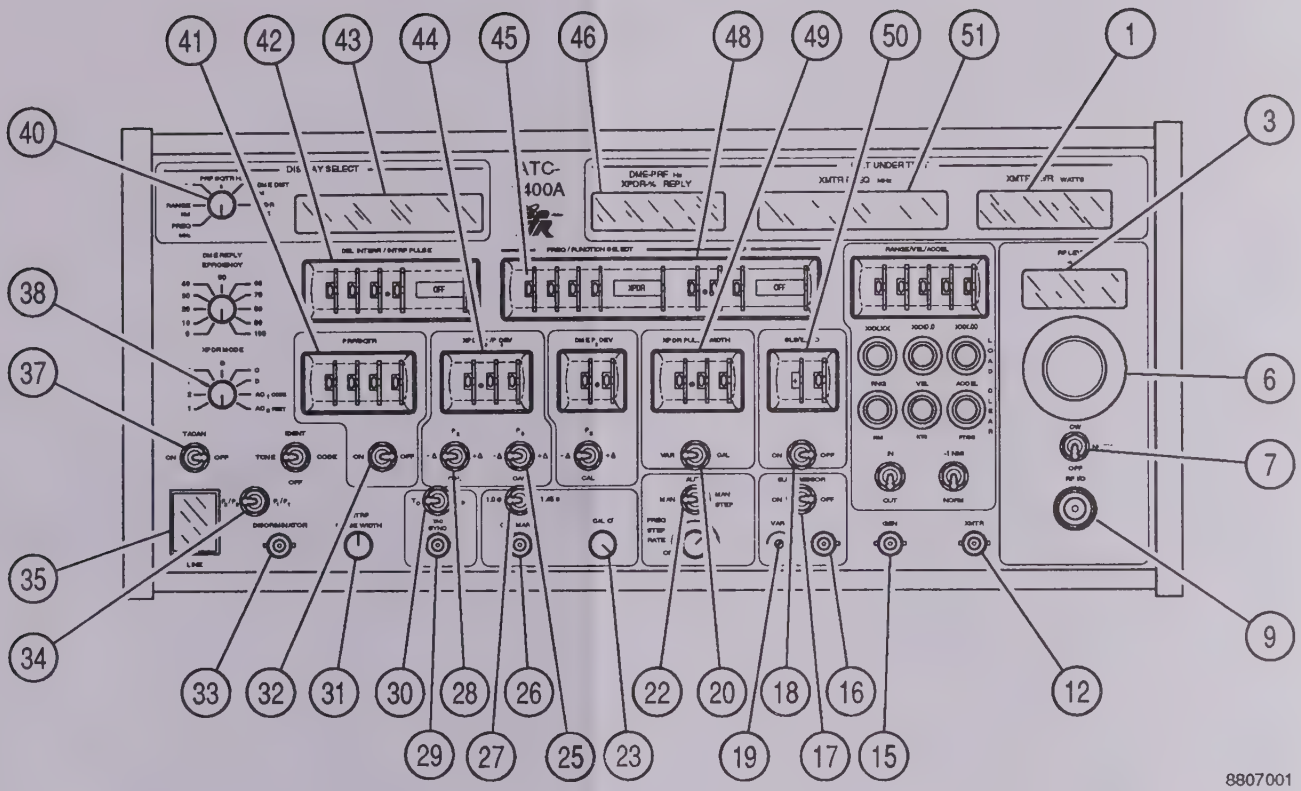
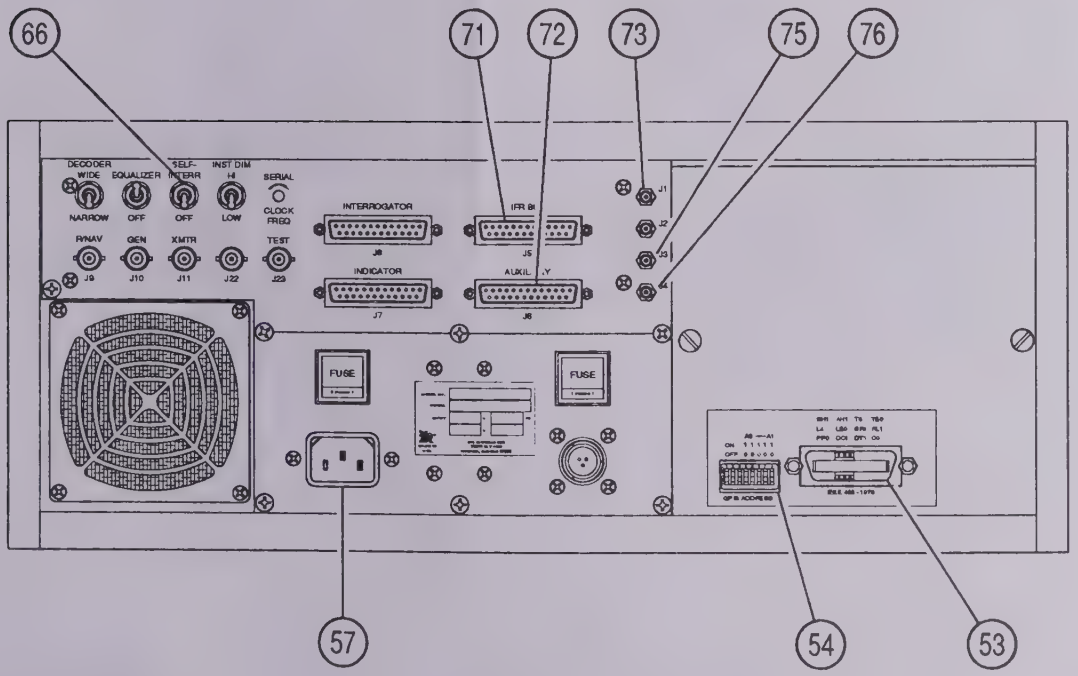
R
Q
P
O
N
M
L
AUXILIARY
PROCESSOR
AC OUT
AC IN
LINE
SELECT

A. CURSOR Keys
B. Keyboard
C. UUT XMTR Connector (J10001)
D. UUT XMTR Indicator
E. ANT B Connector (J10002)
F. SLEW Control
G. POWER Switch
H. BRIGHTNESS Control
I. MENU Display
J. F2 Fuse
K. AC OUT Connector
L. AC IN Connector
M. F1 Fuse
N. LINE SELECT Switch
O. IFR BUS Connector (J10011)
P. DPSK AMPLITUDE BALANCE Adjust (R11026)
Q. TEST Connector (J10012)
R. R12004
S. ANT B REPLY DELAY Adjust (R12005)
T. ANT A REPLY DELAY Adjust (R12006)
U. SPR TIMING Adjust (R12007)
V. R12003
W. ZERO SCALE Adjust (R11023)
X. FULL SCALE Adjust (R11021)
Y. REF VOLTAGE Adjust (R11020)
Z. EXT MOD IN Connector (J10003)
AA. SCOPE TRIG OUT Connector (J10007)
BB. EXT SYNC IN Connector (J10004)
CC. EXT SYNC OUT Connector (J10008)
DD. MODE S/ATCRBS DISCRETE OUT Connector (J10005)
EE. PREPULSE OUT Connector (J10009)
FF. ANT B VIDEO OUT Connector (J10006)
GG. RF VERNIER OUT Connector (J10013)
HH. MEASUREMENT GATE OUT Connector (J10014)
II. DPSK OUT Connector (J10015)
JJ. AUXILIARY Connector (J10010)
KK. 80 MHz Adjust (L11006)

S-1403C Front and Rear Panels
Figure 21




8807001




8807002

XMTR PWR WATTS Display
RF LEVEL -dBm Display
RF LEVEL Control
CW/NORM/OFF Switch
RF I/O Connector (J1015)
XMTR Connector (J1016)
GEN Connector (J1017)
SUPPRESSOR OUTPUT Connector (J1018)
SUPPRESSOR ON/OFF Switch
SLS/ECHO ON/OFF Switch
SUPPRESSOR VAR Adjustment
XPDR PULSE WIDTH VAR/CAL Switch
MAN/AUTO/MAN STEP Switch
CAL Ø Control
XPDR DEV $P_3$/CAL Switch
CAL MARKS Connector (J1019)
1.0 µS/1.45 µS Switch
XPDR DEV $P_2$/CAL Switch
SYNC Connector (J1020)
$T_O$/TAC/$T_D$ Switch
INTRF PULSE WIDTH Control
PRF/SQTR ON/OFF Switch
DISCRIMINATOR Connector (J1021)
$F_2$/$P_2$ $F_1$/$P_1$ Switch
LINE Switch

37. TACAN ON/OFF Switch
38. XPDR MODE Control
40. DISPLAY SELECT Control
41. PRF/SQTR Thumbwheels
42. DBL INTERR/INTRF PULSE Thumbwheels
43. DISPLAY SELECT Readout
44. XPDR $P_2$/$P_3$ DEV Thumbwheels
45. FREQ/FUNCTION SELECT Thumbwheels
46. DME-PRF Hz/XPDR-%REPLY Display
48. ΔF Thumbwheels
49. XPDR PULSE WIDTH Thumbwheels
50. SLS/ECHO Thumbwheels
51. XMTR FREQ MHz Display
53. GPIB Connector
54. GPIB ADDRESS/OPTION Dip Switches
57. AC INPUT Connector
66. SELF-INTERR/OFF Switch
71. IFR BUS Connector (J9105)
72. AUXILIARY Connector (J9102)
73. DABS INPUT Connector (J9101)
75. EXTERNAL MEASUREMENT GATE Connector (J9103)
76. RF LEVEL INPUT Connector (J9104)

ATC-1400A Front and Rear Panels
Figure 22

F. Calibration/Verification Procedures

**NOTE:** When one circuit provides the same pulse characteristic for different pulses, it is necessary to test the specifications for that characteristic only once.

**NOTE:** Pulse spacings are measured from leading edge to leading edge at the 50% amplitude points. Pulse widths are measured from leading edge to trailing edge at the 50% amplitude points.

Refer to 2-2-2, Figure 23 for S-1403C Test and Adjustment Points not shown in 2-2-2, Figure 21. Refer to ATC-1400A Maintenance Manual for ATC-1400A Test and Adjustment Points not shown in 2-2-2, Figure 22.

(1) Power Supply

PREREQUISITES: None

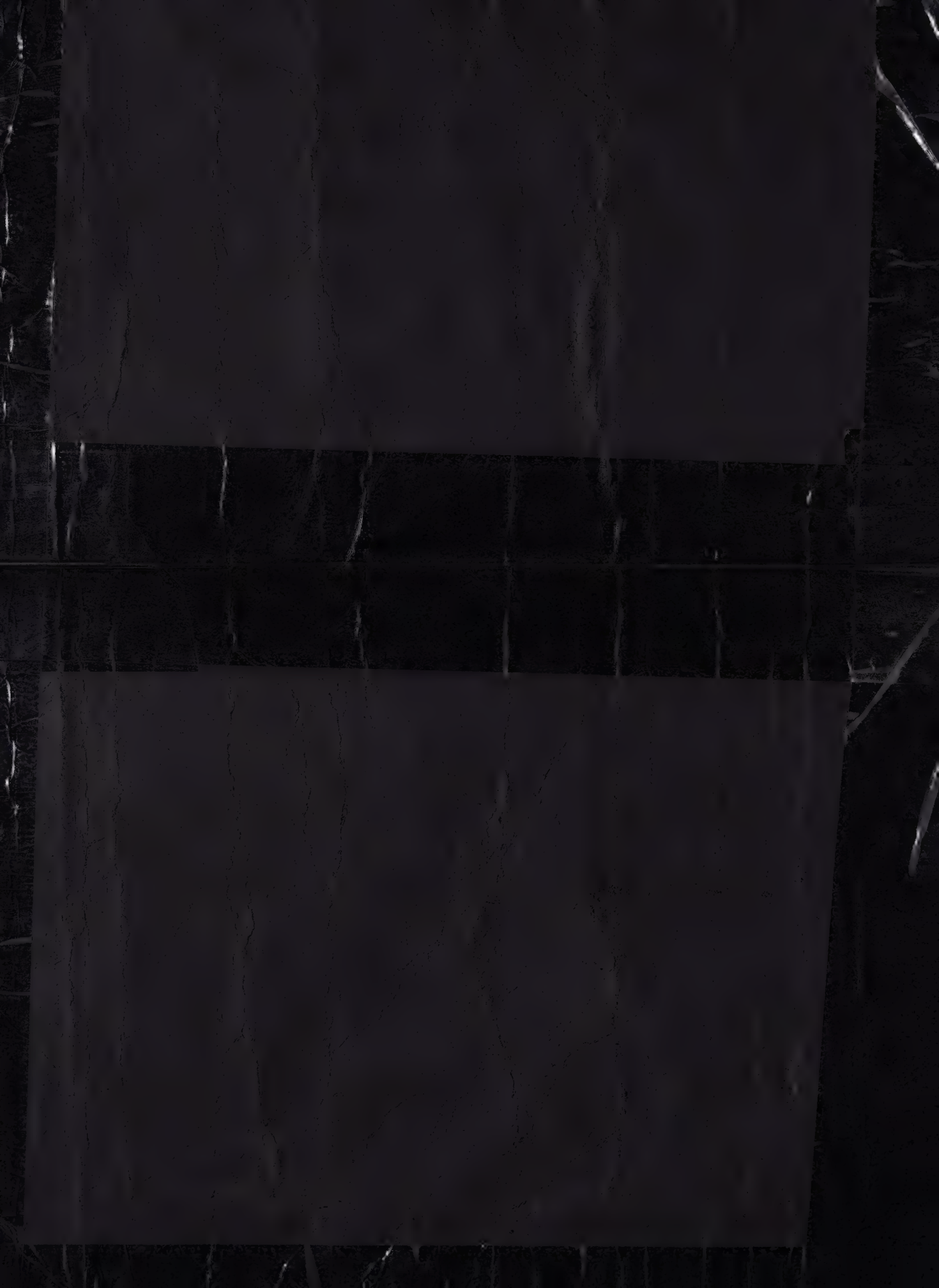
TEST EQUIPMENT: 1 Digital Multimeter

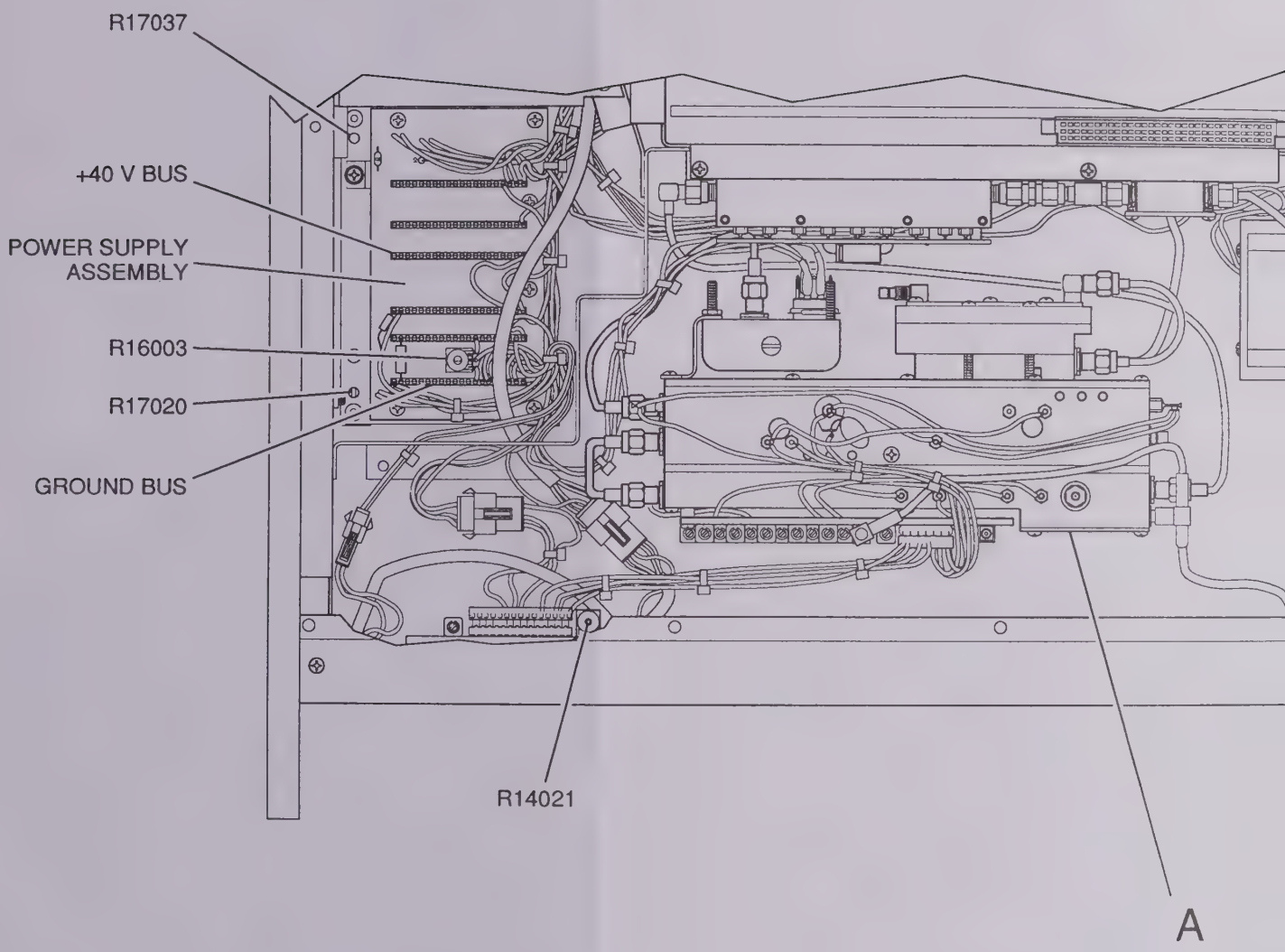
| STEP | PROCEDURE |
|---|---|

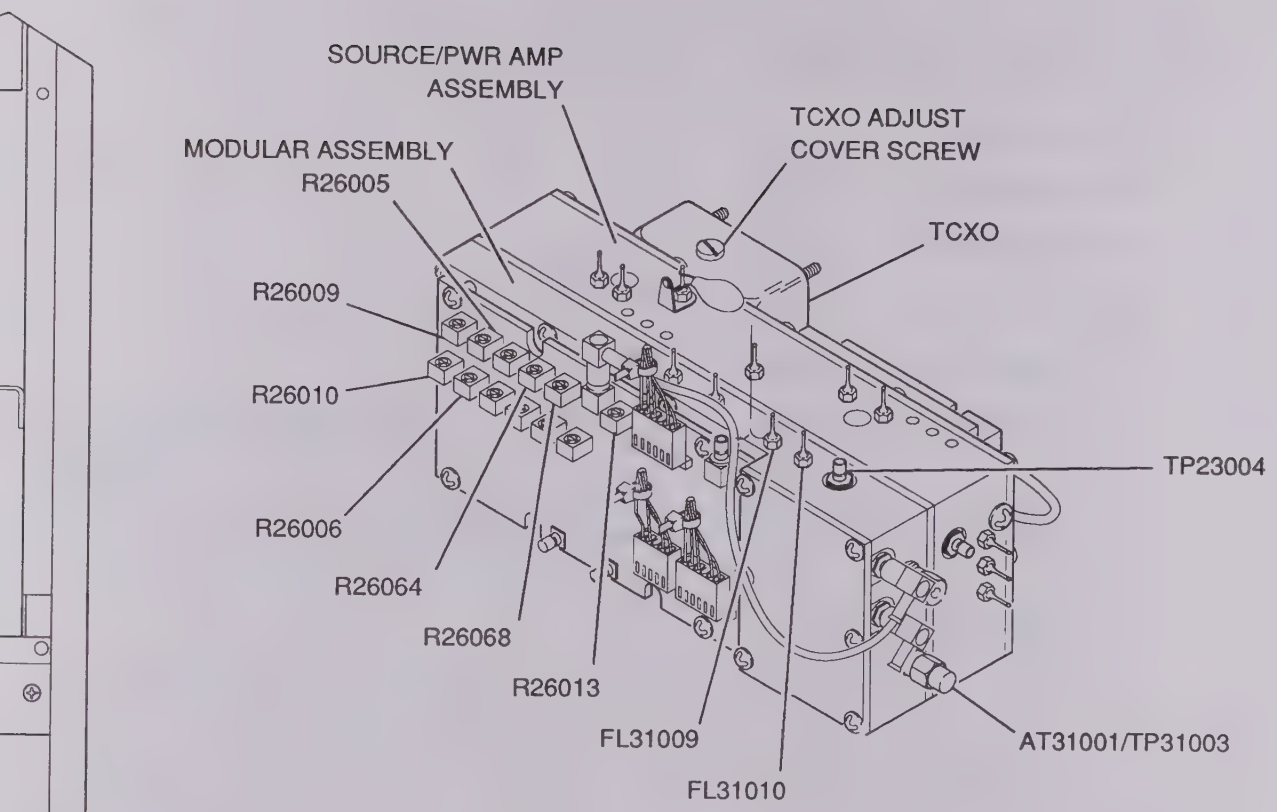
1. Apply power to Mode S Test System.
2. Use Digital Multimeter (DMM) to measure voltage across C11007 on Pulse PC Board Assembly. Refer to Pulse PC Board Assembly drawing.
3. Verify voltage measures +5 Vdc (±0.05 Vdc). If not, adjust R17037 (+5 V Adjust) on Power Supply Assembly to obtain proper level.
4. Use DMM to measure voltage between FL31009 on Modulator Assembly and Ground Bus.
5. Verify voltage measures +12 Vdc (±0.05 Vdc). If not, adjust R17020 (+12 V Adjust) on Power Supply Assembly to obtain proper level.
6. Use DMM to measure voltage between FL31010 on Modulator Assembly and Ground Bus.
7. Verify voltage measures -12 Vdc (±0.25 Vdc). If not, adjust R17020 (+12 V Adjust) on Power Supply Assembly to obtain proper level.
8. Use DMM to measure voltage between +40 V Bus and Ground Bus on Power Supply Assembly.
9. Verify voltage measures +40 Vdc (±5 Vdc). If not, adjust R17020 (+12 V Adjust) on Power Supply Assembly to obtain proper level.

   **NOTE:** If R17020 is adjusted in Steps 7 and/or 9, Steps 4 through 9 must be repeated.

10. Disconnect power from Mode S Test System.




R17037
+40 V BUS
POWER SUPPLY ASSEMBLY
R16003
R17020
GROUND BUS
R14021
A




DIVERSITY MODULE

DETAIL A

8807007

Test Points and Adjustments
Figure 23

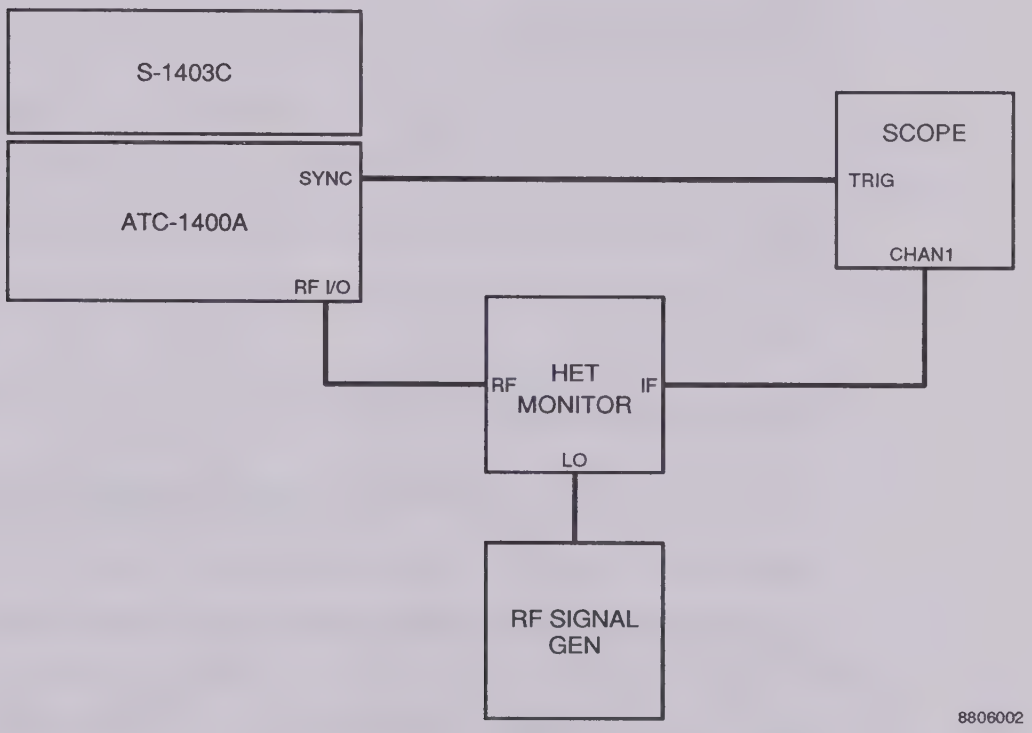
(2) Interrogation Pulses and SPR

This procedure tests the operation of $P_1$, $P_2$, $P_2$ (SLS), $P_3$, $P_4$, $P_5$ (SLS) and $P_6$ Pulses; and SPR.

PREREQUISITES: 2-2-2G(1) Power Supply

TEST EQUIPMENT:
1 Oscilloscope
1 Heterodyne Monitor
1 RF Signal Generator

TEST SETUP DIAGRAM:




Interrogation Pulses and SPR Test Setup Diagram
Figure 24

| STEP | PROCEDURE |
|---|---|

1. Connect Oscilloscope Channel 1 to Heterodyne Monitor IF Connector.
2. Connect Oscilloscope External Trigger to SYNC Connector (29).
3. Connect RF I/O Connector (9) to Heterodyne Monitor RF Connector.
4. Connect RF Signal Generator to Heterodyne Monitor LO Connector.
5. Apply power to Mode S Test System and test equipment.
6. Set RF Signal Generator output for 1030 MHz at +6 dBm.

STEP PROCEDURE

7. Set Mode S Test System as follows:

| CONTROL | | SETTING |
|---|---|---|
| (6) | RF LEVEL Control | ***12*** (-dBm) |
| (7) | CW/NORM/OFF Switch | ***NORM*** |
| (18) | SLS/ECHO ON/OFF Switch | ***OFF*** |
| (20) | XPDR PULSE WIDTH VAR/CAL Switch | ***CAL*** |
| (25) | XPDR DEV $P_3$/CAL Switch | ***CAL*** |
| (28) | XPDR DEV $P_2$/CAL Switch | ***CAL*** |
| (30) | $T_O$/TAC/$T_D$ Switch | ***$T_O$*** |
| (32) | PRF SQUITTER ON/OFF Switch | ***ON*** |
| (38) | XPDR MODE Control | ***A*** |
| (41) | PRF/SQTR Thumbwheels | ***200*** |
| (45) | FREQ/FUNCTION SELECT Thumbwheels | ***1030 XPDR*** |
| (50) | SLS ECHO Thumbwheels | ***-0*** |
| (I) | MENU Display (Control Menu #1) | ***Func: (1) ATC*** |

8. Adjust Vertical Vernier Control on Oscilloscope for full display of $P_1$ pulse.

9. Verify $P_1$ pulse rise and fall time, from 10% point to 90% point, is 70 ns (±20 ns).

10. Using Oscilloscope Δtime start and stop controls, overlay leading and trailing edge of $P_1$ pulse at 50% point.

11. Verify $P_1$ pulse width is 0.80 µs (±10 ns). If not, adjust R2603 (XPDR Pulse Width Adjust) on ATC-1400A RF Control PC Board Assembly.

12. Set XPDR PULSE WIDTH VAR/CAL Switch (20) to ***VAR***.

13. Set XPDR PULSE WIDTH Thumbwheels (49) to ***0.20*** µs. Verify $P_1$ pulse width is 0.20 µs (±10 ns).

14. Set XPDR PULSE WIDTH Thumbwheels (49) to ***1.85*** µs. Verify $P_1$ pulse width is 1.85 µs (±10 ns).

15. Set XPDR PULSE WIDTH VAR/CAL Switch (20) to ***CAL***.

16. Verify XPDR pulse spacing, displayed on Oscilloscope for each XPDR MODE Control (38) setting, as follows:

| POSITION | PULSE SPACING |
|---|---|
| Mode ***1*** | 3.00 µs (±10 ns) |
| Mode ***2*** | 5.00 µs (±10 ns) |
| Mode ***T*** | 6.50 µs (±10 ns) |
| Mode 3/***A*** | 8.00 µs (±10 ns) |
| Mode ***B*** | 17.00 µs (±10 ns) |
| Mode ***C*** | 21.00 µs (±10 ns) |
| Mode ***D*** | 25.00 µs (±10 ns) |

17. Set XPDR MODE Control (38) to ***A***.

| STEP | PROCEDURE |
|---|---|

18. Verify $P_3$ pulse width is 0.8 µs (±10 ns).

19. Set ***Func: (3) ACS***. Verify $P_1$ to $P_3$ pulse spacing is 8.0 µs (±10 ns).

20. Verify $P_1$ to $P_4$ pulse spacing is 10.0 µs (±10 ns).

21. Verify ***P4:,Wd= CAL***. Verify $P_4$ pulse width is 0.8 µs (±10 ns).

22. Position cursor to ***P4:,Wd=***. Press ON/CAL Key. Verify numerical value is displayed.

23. Using SLEW Control (F), verify $P_4$ pulse width varies from 200 ns (±10 ns) to 2.75 µs (±10 ns).

24. Press ON/CAL Key.

25. Set ***Func: (4) ACL***. Verify $P_1$ to $P_3$ pulse spacing is 8.0 µs (±10 ns).

26. Verify $P_1$ to $P_4$ pulse spacing is 10.0 µs (±10 ns).

27. Position cursor to ***P4:,Wd=***. Verify $P_4$ pulse width is 1.6 µs (±10 ns).

28. Press ON/CAL Key. Verify numerical value is displayed.

29. Using SLEW Control (F), verify $P_4$ pulse width varies from 200 ns (±10 ns) to 3.55 µs (±10 ns).

30. Set XPDR MODE Control (38) to ***C***.

31. Verify $P_1$ to $P_3$ pulse spacing is 21.0 µs (±10 ns).

32. Verify $P_1$ to $P_4$ pulse spacing is 23.0 µs (±10 ns).

33. Set ***Func: (3) ACS***. Verify $P_1$ to $P_3$ spacing is 21.0 µs (±10 ns).

34. Verify $P_1$ to $P_4$ pulse spacing is 23.0 µs (±10 ns).

35. Set ***Func: (1) ATC***.

36. Set XPDR $P_2/P_3$ DEV Thumbwheels (44) to ***1.85***.

37. Set XPDR DEV $P_3$/CAL Switch (25) to ***+Δ***. Verify $P_1$ to $P_3$ pulse spacing is 22.85 µs (±10 ns).

38. Set XPDR DEV $P_3$/CAL Switch (25) to ***-Δ***. Verify $P_1$ to $P_3$ pulse spacing is 19.15 µs (±10 ns).

39. Set XPDR $P_3$/CAL Switch (25) to ***CAL***.

40. Set SLS/ECHO ON/OFF Switch (18) to ***ON***.

41. Set SLS/ECHO Thumbwheels (50) to ***+5***.

STEP PROCEDURE

42. Verify $P_2$ has shifted +5 dB (±0.5 dB) from $P_1$.

43. Set SLS/ECHO ON/OFF Switch (18) to ***OFF***.

44. Set ***P3:VAR***.

45. Set SLS/ECHO Thumbwheels (50) to ***-19***.

46. Verify $P_3$ has shifted -19 dB (±0.5 dB) from $P_1$.

47. Set SLS/ECHO Thumbwheels (50) to ***-10***.

48. Verify $P_3$ is -10 dB (±0.3 dB) relative to $P_1$.

49. Set SLS/ECHO Thumbwheels (50) to ***+6***.

50. Verify $P_3$ has shifted +6 dB (±0.5 dB) relative to $P_1$.

51. Set SLS/ECHO Thumbwheels (50) to ***00***.

52. Verify $P_3$ amplitude is 0.0 dB (±0.3 dB) relative to $P_1$.

53. Set ***P3:CAL***.

54. Set ***Func: (2) SEQ***.

55. Press SMENU Key.

56. Use SLEW Control (F) to change to Sequence Menu S02. Press ON/CAL Key to set ***S02:OFF***.

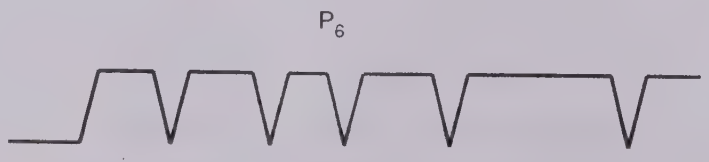
57. Repeat Step 56 for Sequence Menus S03 through S08.

58. Use SLEW Control (F) to return to Sequence Menu S01.

59. Set ***UF# 04*** and ***ADD=17725762***.

60. Verify $P_6$ has level amplitude peaks according to 2-2-2, Figure 25. If not, adjust R11026 (DPSK AMPLITUDE BALANCE Adjust [P]) on Pulse PC Board Assembly, to level peaks.

61. Set ***UF#16***. Verify $P_6$ width is 30.25 µs (±10 ns).




$P_6$ Amplitude Example
Figure 25

| STEP | PROCEDURE |
|---|---|

62. Set ***UF#00***. Verify $P_6$ width is 16.25 µs (±10 ns).

63. Press CMENU and "1" Keys in sequence. Verify Control Menu #1 with ***Func: (2) SEQ*** is displayed.

64. Verify $P_1$ to $P_6$ pulse spacing is 3.5 µs (±10 ns).

65. Position cursor to ***P6:,Wd=*** field.

66. Press ON/CAL Key. Verify numerical value is displayed.

67. Using SLEW Control (F), verify $P_6$ width varies from 14.75 µs (±10 ns) to 17.75 µs (±10 ns) in 50 ns steps from CAL position.

68. Verify $P_1$ to $P_2$ pulse spacing is 2.0 µs (±10 ns).

69. Verify $P_2$ pulse width is 0.80 µs (±10 ns).

70. Set ***P6:OFF***.

71. Set XPDR DEV $P_2$/CAL Switch (28) to +Δ. Set XPDR $P_2$/$P_3$ Thumbwheels (44) to ***1.85***. Verify $P_1$ to $P_2$ pulse spacing is 3.85 µs (±10 ns).

72. Set XPDR DEV $P_2$/CAL Switch (28) to -Δ. Verify $P_1$ with $P_2$ merged pulse width is 0.15 µs + $P_2$ pulse width in Step 69 (±10 ns). (Actual $P_1$ to $P_2$ pulse spacing is measured value minus $P_2$ pulse width.)

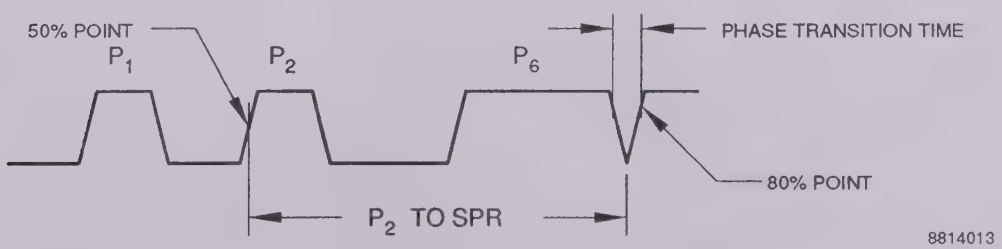
73. Set XPDR DEV $P_2$/CAL Switch (28) to ***CAL***.

74. Set ***P6:CAL***.

75. Verify SYNC PHASE REVERSAL (SPR) occurs 2.75 µs (±10 ns) following leading edge of $P_2$. Refer to 2-2-2, Figure 26. If not, adjust R12007 (SPR TIMING Adjust [U]) on Processor PC Board Assembly.

    **NOTE:** If SPR cannot be adjusted to within tolerance, reset JTB11001 on Pulse PC Board Assembly. Refer to 2-2-2, Figure 30.

76. Verify SPR and all $P_6$ phase transition times are less than 80 ns at 80% points.




$P_2$ to SPR Spacing/Phase Transition Time
Figure 26

| STEP | PROCEDURE |
|---|---|

77. Position cursor to ***SPR:Dv=*** field. Press ON/CAL Key. Verify numerical value is displayed.

78. Using SLEW Control (F), verify SPR occurs from 1.75 µs (±10 ns) to 3.75 µs (±10 ns) following leading edge of $P_2$.

79. Set ***SPR:Dv=CAL***.

80. Set SLS/ECHO ON/OFF Switch (18) to ***ON***.

81. Set ***P6:OFF***.

82. Using Oscilloscope Δtime start control, center 50% point of leading edge of $P_5$ on Major Vertical.

83. Set SLS/ECHO ON/OFF Switch (18) to ***OFF***.

84. Set ***P6:CAL***.

85. Using Oscilloscope Δtime stop control, center SPR on Major Vertical. Verify Δtime reading ($P_5$ leading edge to SPR) is 400 ns (±100 ns).

86. Using Oscilloscope Δtime start control, center SPR on Major Vertical.

87. Set ***P6:OFF***.

88. Set SLS/ECHO ON/OFF Switch (18) to ***ON***.

89. Using Oscilloscope Δtime stop control, center 50% point of $P_5$ trailing edge on Major Vertical. Verify Δtime reading (SPR to $P_5$ trailing edge) is 400 ns (±100 ns).

90. Add readings from Steps 85 and 89 together and verify $P_5$ pulse width is 800 ns (±100 ns).

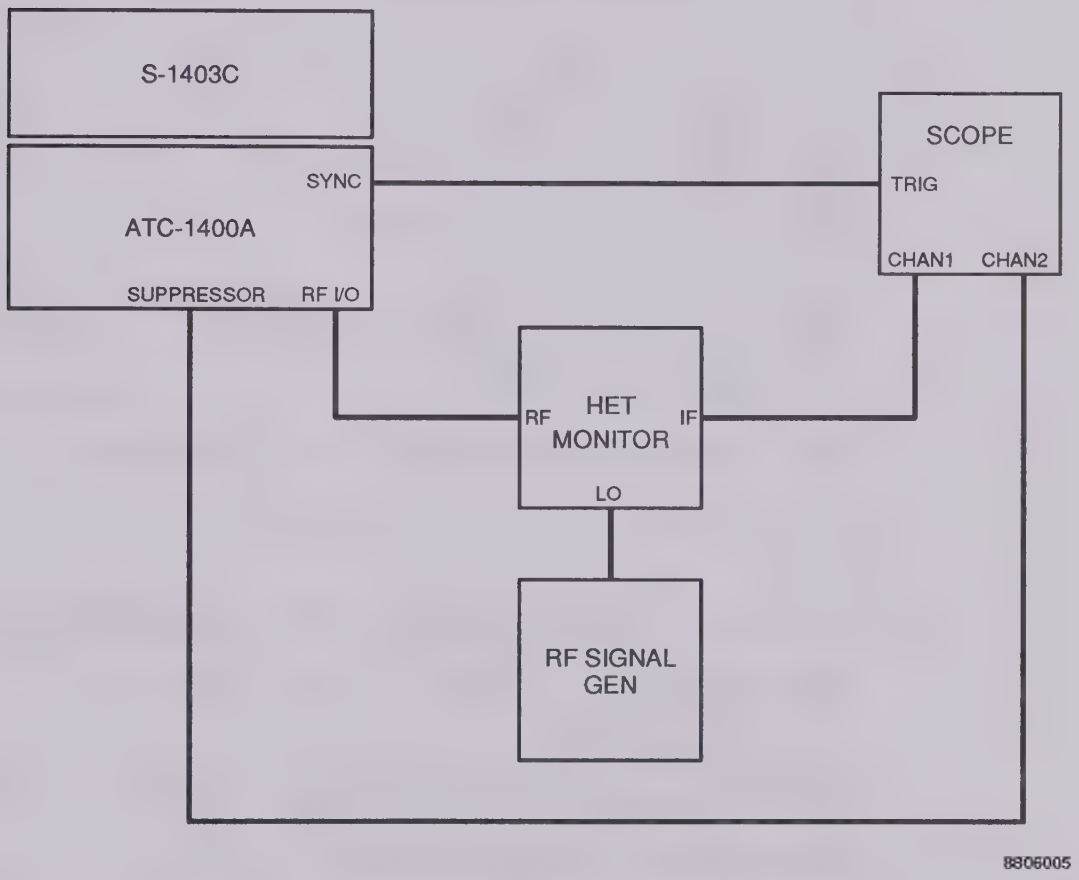
91. Remove power and disconnect test equipment.

(3) Suppressor and Interference Pulses

PREREQUISITES: 2-2-2G(1) Power Supply

TEST EQUIPMENT:
1 Oscilloscope
1 Heterodyne Monitor
1 RF Signal Generator

TEST SETUP DIAGRAM:




Suppressor and Interference Pulses Test Setup Diagram
Figure 27

| STEP | PROCEDURE |
|---|---|

1. Connect Oscilloscope Channel 1 to Heterodyne Monitor IF Connector.
2. Connect Oscilloscope External Trigger to SYNC Connector (29).
3. Connect Oscilloscope Channel 2 to SUPPRESSOR OUTPUT Connector (16).
4. Connect RF I/O Connector (9) to Heterodyne Monitor RF Connector.

STEP PROCEDURE

5. Connect RF Signal Generator to Heterodyne LO Connector.

6. Apply power to Mode S Test System and test equipment.

7. Set RF Signal Generator output for 1030 MHz at +6 dBm.

8. Set Mode S Test System as follows:

| CONTROL | | SETTING |
|---|---|---|
| (6) | RF LEVEL Control | ***12*** (-dBm) |
| (7) | CW/NORM/OFF Switch | ***NORM*** |
| (18) | SLS/ECHO ON/OFF Switch | ***OFF*** |
| (20) | XPDR PULSE WIDTH VAR/CAL Switch | ***CAL*** |
| (30) | $T_O$/TAC/$T_D$ Switch | ***$T_O$*** |
| (32) | PRF SQUITTER ON/OFF Switch | ***ON*** |
| (38) | XPDR MODE Control | ***A*** |
| (41) | PRF/SQTR Thumbwheels | ***200*** |
| (42) | DBL INTERR/INTRF PULSE Thumbwheels | ***017.5 INTERF-*** |
| (45) | FREQ/FUNCTION SELECT Thumbwheels | ***1030 XPDR*** |
| (50) | SLS ECHO Thumbwheels | ***-0*** |
| (I) | MENU Display | ***Func: (1) ATC*** |

9. Adjust Oscilloscope Vertical Vernier Control for full display of $P_1$ pulse.

10. Verify an interference pulse is positioned 17.5 µs (±0.0509 µs) prior to $P_1$.

11. Set DBL INTERR/INTRF PULSE Thumbwheels (42) to ***399.0 INTERF+***. Verify pulse is positioned 399 µs (±0.07 µs) after leading edge of $P_1$.

    **NOTE**: Oscilloscope errors may contribute significantly to accuracy of this measurement.

12. Rotate INTRF PULSE WIDTH Control (31) fully ccw and cw. Verify pulse width can be adjusted from 0.2 to 5.0 µs.

13. Set ***Func: (6) DI, 1st=ATC, 2nd=ATC***.

14. Set DBL INTERR/INTRF PULSE Thumbwheels (42) to ***200.0 DOUBLE***. Verify leading edge of $P_1$ in second interrogation is positioned 200 µs (±50 ns) after leading edge of $P_1$ in first interrogation.

15. Set SUPPRESSOR ON/OFF Switch (17) to ***ON***. Verify suppression pulse removes first interrogation and shifts second interrogation by mode spacing.

16. Set DBL INTERR/INTRF PULSE Thumbwheels (42) to ***000.0 OFF***.

17. Set ***Func: (1) ATC***.

18. Verify suppression pulse occurs 800 ns (±100 ns) prior to $P_3$.

| STEP | PROCEDURE |
|---|---|

19. Set ***Func: (2) SEQ***. Verify pulse occurs 800 ns (±100 ns) prior to SPR.
20. Set ***Func: (3) ACS***. Verify pulse occurs 800 ns (±100 ns) prior to $P_3$.
21. Set ***Func: (4) ACL***. Verify pulse occurs 800 ns (±100 ns) prior to $P_3$.
22. Remove power and disconnect test equipment.

(4) RF Level

PREREQUISITES: 2-2-2G(1) Power Supply

TEST EQUIPMENT: 1 Spectrum Analyzer
1 Power Meter

TEST SETUP DIAGRAM: None

STEP PROCEDURE

1. Apply power to Mode S Test System and test equipment.

2. Set Mode S Test System as follows:

| CONTROL | | SETTING |
|---|---|---|
| (6) | RF LEVEL Control | ***00*** (-dBm) |
| (7) | CW/NORM/OFF Switch | ***CW*** |
| (18) | SLS/ECHO ON/OFF Switch | ***OFF*** |
| (22) | MAN/AUTO/MAN STEP Switch | ***MAN*** |
| (32) | PRF SQUITTER ON/OFF Switch | ***ON*** |
| (38) | XPDR MODE Control | ***2*** |
| (41) | PRF/SQTR Thumbwheels | ***1200*** |
| (45) | FREQ/FUNCTION SELECT Thumbwheels | ***1030 XPDR*** |
| (49) | XPDR PULSE WIDTH Thumbwheels | ***1.85*** |
| (I) | MENU Display | ***RFLvl:+0.0*** |

3. Connect Power Meter to RF I/O Connector (9).

4. Disconnect cable from J10013 on rear panel of S-1403C.

5. Record Power Meter reading for reference.

6. Reconnect cable to J10013. Verify power reading changes less than 0.05 dB. If not, adjust R11023 (ZERO SCALE Adjust [W]) on Pulse PC Board Assembly to reference level from Step 5.

7. Set ***RFLvl:+3.0*** and verify increase of 3.0 dB (±0.3 dB) from Step 5 reference level. If not, adjust R11021 (FULL SCALE Adjust [X]) on Pulse PC Board Assembly.

8. Set ***RFLvl:-3.0*** and verify decrease of 3.0 dB (±0.3 dB) from Step 5 reference level. If not, adjust R11021 (FULL SCALE Adjust [X]).

9. Set ***RFLvl:+0.0*** and verify reference level (±0.05 dB). If not, or if any adjustments were made in Steps 7 or 8, repeat Steps 6 through 9 until no adjustments are necessary.

10. Rotate RF LEVEL Control (6) until ***50*** (-dBm) or ***20*** (-dBm) (if MLD option is installed) is displayed on RF LEVEL -dBm Display (3).

11. Disconnect Power Meter from RF I/O Connector (9).

12. Connect Spectrum Analyzer to RF I/O Connector (9).

STEP PROCEDURE

13. Set CW/NORM/OFF Switch (7) to ***NORM***.

14. Set Spectrum Analyzer to Zero Span, with widest possible IF and VIDEO Filters selected. Adjust Spectrum Analyzer trigger for stable display of $P_1$ and $P_3$.

15. Record signal level on Spectrum Analyzer for reference.

16. Connect ANT B Connector (E) to Spectrum Analyzer.

17. Verify signal level equals reference level noted in Step 15 (±1 dB). If not, adjust R26013 (RF Level Adjust) on Modulator Assembly.

    **NOTE:** Steps 18 through 27 only apply if MLD option is installed.

18. Set CW/NORM/OFF Switch (7) to ***CW***.

19. Disconnect Spectrum Analyzer from ANT B Connector (E).

20. Connect Power Meter to ANT B Connector (E).

21. Press C MENU and "2" Keys in sequence. Verify Control Menu #2 is displayed.

22. Set ***Brf= -20 dBm*** and ***Brflv=+0.0 dB***. Verify Power Meter reading is -20 dBm (±1 dB). Record signal level for a reference.

23. Set ***Brflv=+3.0 dB***. Verify Power Meter reading is reference level from Step 22 + 3.0 dB (±0.3 dB). If not, adjust R14021 on Front Panel Processor PC Board Assembly.

24. Set ***Brflv=-0.0 dB***. Verify Power Meter reading is reference level from Step 22 (±0.05 dB). If not, adjust R26013 (RF Level Adjust) on Modulator Assembly.

25. Repeat Steps 23 and 24 until no adjustments are required.

26. Set ***Brflv=-3.0 dB***. Verify Power Meter reading is reference level from Step 22 - 3.0 dB (±0.3 dB).

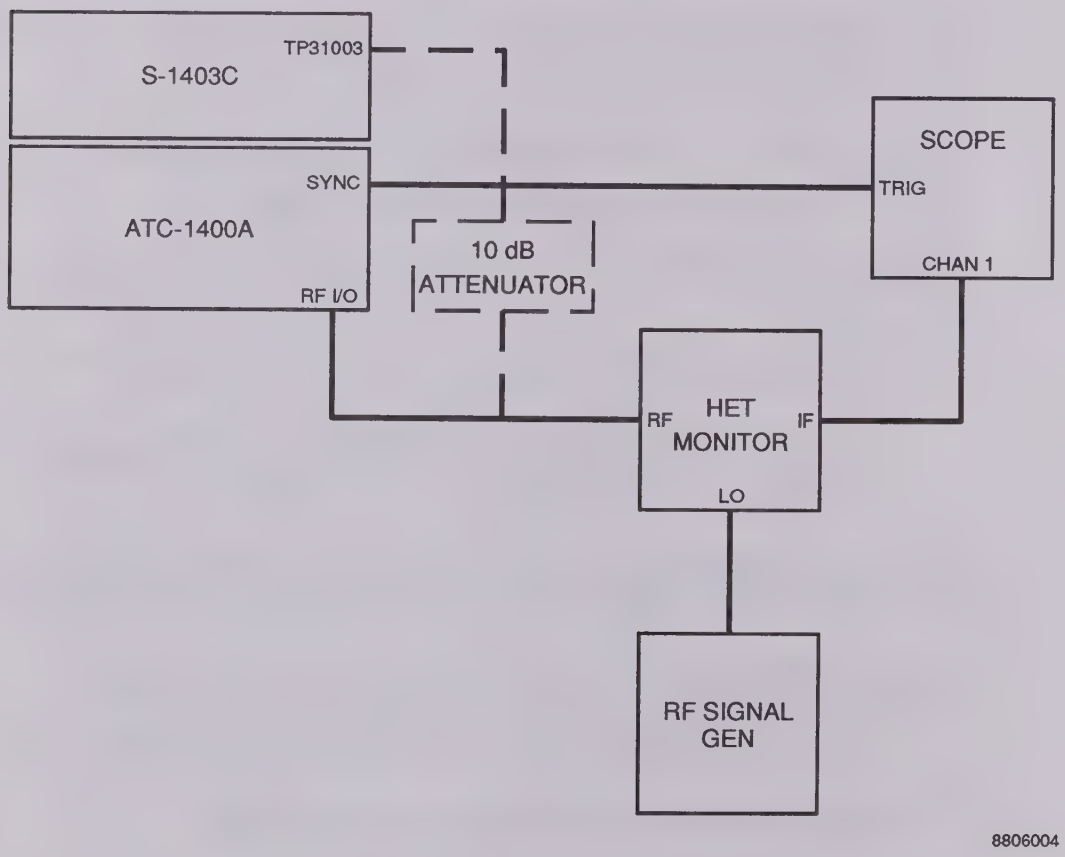
27. Remove power and disconnect test equipment.

(5) Antenna B

PREREQUISITES: 2-2-2G(1) Power Supply
2-2-2G(4) RF Level

TEST EQUIPMENT:
1 10 dB Attenuator (only if MLD option is installed)
1 Oscilloscope
1 Heterodyne Monitor
1 Frequency Counter
1 RF Signal Generator
1 DMM

TEST SETUP DIAGRAM:




Antenna B Test Setup Diagram
Figure 28

| STEP | PROCEDURE |
|---|---|

1. Connect Oscilloscope External Trigger to SYNC Connector (29).

2. Connect Oscilloscope Channel 1 to Heterodyne Monitor IF Connector.

STEP PROCEDURE

3. Connect Heterodyne Monitor RF Connector to RF I/O Connector (9).

4. Connect RF Signal Generator to Heterodyne Monitor LO Connector.

5. Apply power to Mode S Test System and test equipment.

6. Set RF Signal Generator output for 1030 MHz at +6 dBm.

7. Set Mode S Test System as follows:

| CONTROL | | SETTING |
|---|---|---|
| (7) | CW/NORM/OFF Switch | ***NORM*** |
| (18) | SLS/ECHO ON/OFF Switch | ***OFF*** |
| (20) | XPDR PULSE WIDTH VAR/CAL Switch | ***CAL*** |
| (21) | FREQ STEP RATE Control | ***OFF*** |
| (22) | MAN/AUTO/MAN STEP Switch | ***MAN*** |
| (25) | XPDR DEV $P_3$/CAL Switch | ***CAL*** |
| (28) | XPDR DEV $P_2$/CAL Switch | ***CAL*** |
| (30) | $T_O$/TAC/$T_D$ Switch | ***To*** |
| (32) | PRF SQUITTER ON/OFF Switch | ***ON*** |
| (38) | XPDR MODE Control | ***A*** |
| (41) | PRF/SQTR Thumbwheels | ***200*** |
| (45) | FREQ/FUNCTION SELECT Thumbwheels | ***1030 XPDR*** |
| (50) | SLS ECHO Thumbwheels | ***-0*** |
| (I) | MENU Display | ***Func: (1) ATC*** |

8. Press SMENU Key.

9. Use SLEW Control (F) to select Sequence Menu S02. Press ON/CAL Key to set ***S02:OFF***.

10. Repeat Step 9 for Sequence Menus S03 through S08.

11. Press 2nd, FUN NO and "2" Keys in sequence.

12. Set Oscilloscope for 2 µs/Div resolution. Use Oscilloscope Δtime to record time from sync to $P_1$ of ATC-1400A.

13. Set ***AntB: ON***.

14. Remove AT31001 termination and connect Heterodyne Monitor RF IN to TP31003 on Modulator Assembly. If MLD option is not installed, go to Step 27. If MLD option is installed, connect 10 dB Attenuator between Heterodyne Monitor and the S-1403C.

    **NOTE:** Steps 15 through 26 only apply if MLD option is installed.

15. Press CMENU and "2" Keys in sequence.

16. Set ***Brflv=+3.0 dB***.

17. Adjust Oscilloscope for full screen display.

STEP PROCEDURE

18. Align leading edge of $P_1$ with major vertical on Oscilloscope.

19. Set ***BrfIv=-3.0 dB***.

20. Adjust Oscilloscope for full screen display.

21. Verify leading edge of $P_1$ is aligned with same major vertical in Step 18. If not, adjust R26068 on Modulator Assembly.

22. Set ***BrfIv=+3.0 dB***.

23. Adjust Oscilloscope for full screen display.

24. Verify leading edge of $P_1$ is aligned with same major vertical in Step 21. If not, adjust R26064 on Modulator Assembly.

25. Repeat Steps 19 through 24 until no adjustments are required. (Difference between $P_1$ positions at both level settings is ≤10 ns).

26. Set ***BrfIv=+0.0 dB***.

27. Adjust Oscilloscope for full screen display.

28. Use Oscilloscope Δtime to verify time from sync to $P_1$ is equal to time recorded in Step 12 (±25 ns). If not, adjust R26010 on Modulator Assembly.

    **NOTE:** If sync to $P_1$ spacing cannot be adjusted to within tolerance, reset JTB11002 on Pulse PC Board Assembly. Refer to 2-2-2, Figure 30. Readjust R26010 on Modulator Assembly after resetting JTB11002.

29. Verify $P_1$ has a pulse width of 800 ns (±10 ns). If not, adjust R26009 on Modulator Assembly.

30. Verify SPR occurs 2.75 µs (±10 ns) following leading edge of $P_2$. If not, adjust R26006 on Modulator Assembly.

    **NOTE:** If SPR cannot be adjusted to within tolerance, reset JTB11003 on Pulse PC Board Assembly. Refer to 2-2-2, Figure 30. Readjust R26006 on Modulator Assembly after resetting JTB11003.

31. If R26006 was adjusted in Step 30, adjust R26005 on Modulator Assembly to set time from SPR to second phase transition at 1.0 µs (±10 ns).

32. Press ON/CAL Key. Use SLEW Control (F) to set ***AntB=+0.95***. Press ENT Key.

33. Verify $P_1$ pulse has shifted +950 ns (±50 ns) from position in Step 28.

34. Press +/- Key. Verify $P_1$ pulse has shifted -950 ns (±50 ns) from position in Step 28.

STEP PROCEDURE

35. Set CW/NORM/OFF Switch (7) to ***CW***.

36. Disconnect Heterodyne Monitor from TP31003 or 10 dB Attenuator, if MLD option is installed.

37. Connect Frequency Counter to TP31003 on Modulator Assembly or 10 dB Attenuator, if MLD option is installed.

38. Verify frequency measured is 1030 MHz (±10 kHz). If correct, this concludes Antenna B procedure. If incorrect, continue with Step 39.

    **NOTE**: If measured frequency is more than 20 kHz out of tolerance, contact IFR Customer Service for further instructions.

39. Use DMM to verify voltage between R16003 wiper on Power Supply Assembly and Ground Bus is 6.0 Vdc (±0.5 Vdc). If not, adjust R16003 to proper voltage level.

40. Set course adjustment on TCXO (underneath TCXO Adjust Cover Screw) for 1030 MHz (±400 Hz).

41. Readjust R16003 to set frequency at 1030 MHz (±50 Hz).

42. Remove power and disconnect test equipment.

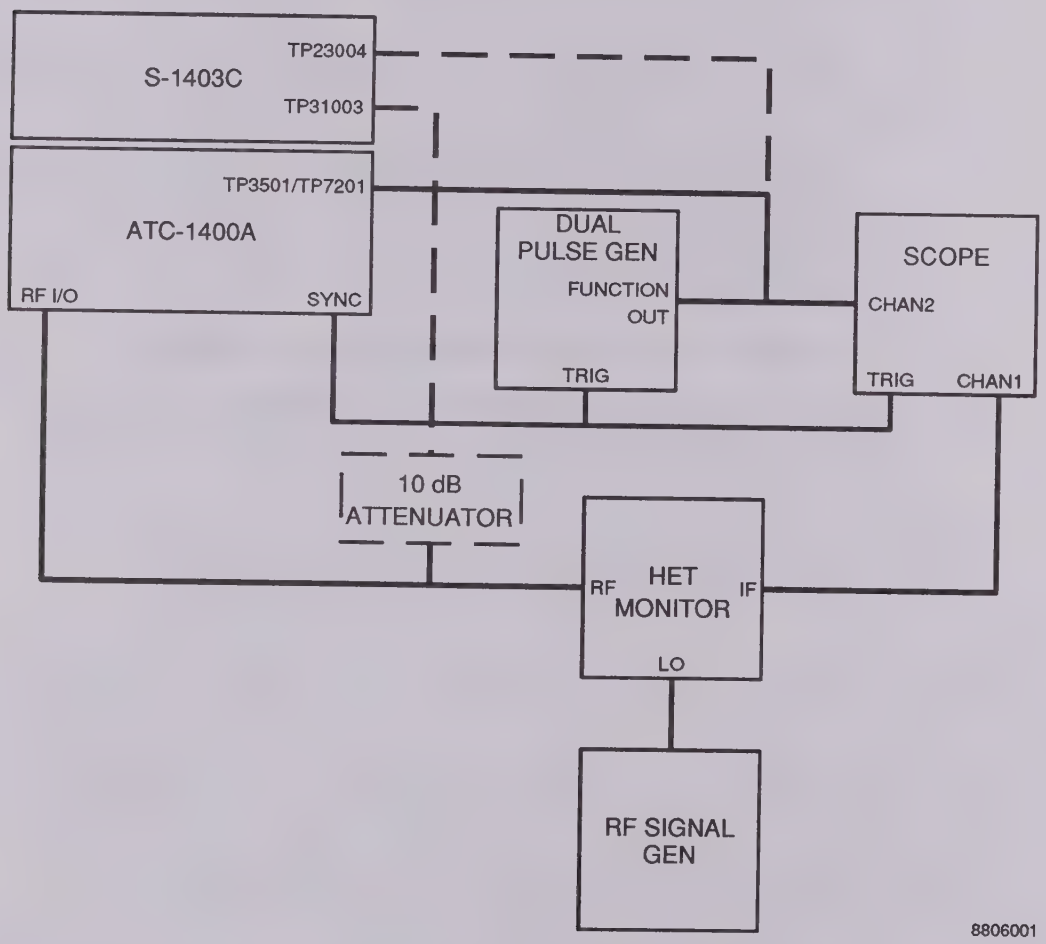
43. Reconnect AT31001 termination to TP31003.

(6) Reply Delay and PPMG

PREREQUISITES: 2-2-2G(1) Power Supply

TEST EQUIPMENT:
1 10 dB Attenuator (only if MLD option is installed)
1 Oscilloscope
1 Heterodyne Monitor
1 Dual Pulse Generator
1 RF Signal Generator

TEST SETUP DIAGRAM:




Reply Delay and PPG Test Setup Diagram
Figure 29

| STEP | PROCEDURE |
|---|---|

1. Connect Oscilloscope External Trigger and Dual Pulse Generator Trigger to SYNC Connector (29).

2. Connect Oscilloscope Channel 1 to Heterodyne Monitor IF Connector.

STEP PROCEDURE

3. Connect Heterodyne Monitor RF Connector to RF I/O Connector (9).

4. Connect RF Signal Generator to Heterodyne Monitor LO Connector.

5. Set Mode S Test System as follows:

| CONTROL | | SETTING |
|---|---|---|
| (7) | CW/NORM/OFF Switch | ***NORM*** |
| (18) | SLS/ECHO ON/OFF Switch | ***OFF*** |
| (20) | XPDR PULSE WIDTH VAR/CAL Switch | ***CAL*** |
| (22) | MAN/AUTO/MAN STEP Control | ***MAN*** |
| (25) | XPDR DEV $P_3$/CAL Switch | ***CAL*** |
| (30) | $T_O$/TAC/$T_D$ Switch | ***$T_O$*** |
| (32) | PRF SQUITTER ON/OFF Switch | ***ON*** |
| (38) | XPDR MODE Control | ***A*** |
| (41) | PRF/SQTR Thumbwheels | ***200*** |
| (45) | FREQ/FUNCTION SELECT Thumbwheels | ***1030 XPDR*** |
| (I) | MENU Display | ***Func: (1) ATC*** |

6. Remove 50 Ω Termination from TP3501/TP7201 on ATC-1400A Video Detector PC Board Assembly. Connect Dual Pulse Generator to TP7201/TP3501 and Oscilloscope Channel 2.

7. Apply power to Mode S Test System and test equipment.

8. Set RF Signal Generator output for 1030 MHz at +6 dBm.

9. Set Pulse Generator for 20.3 µs two pulse (negative polarity) reply.

10. Set delay between $P_3$ and $F_1$ to approximately 3.0 µs.

11. Adjust Pulse Generator Amplitude for an approximate 100 W and note reading on XMTR PWR WATTS Display (1).

12. Use Oscilloscope Δtime to measure delay time between $P_3$ and $F_1$.

13. Verify ***RpDly:*** field value equals Δtime reading (±100 ns). If not, adjust R12006 (ANT A REPLY DELAY Adjust [T]).

14. Set $F_2/P_2$ $F_1/P_1$ Switch (34) to ***$F_2/P_2$***. Verify XMTR PWR WATTS Display (1) has not changed from value in Step 11.

15. Press 2nd and PPG Keys in sequence. Using SLEW Control (F), select ***$f_2$*** in ***Pulse Power Gate:*** field.

16. Verify value displayed in XMTR PWR WATTS Display (1) has not changed greater than 10% from value in Step 14.

17. Use SLEW Control (F) to select ***spl*** in ***Pulse Power Gate:*** field.

18. Verify XMTR POWER WATTS Display (1) reads ***0***.

| STEP | PROCEDURE |
|---|---|

19. Disconnect Dual Pulse Generator from TP3501/TP7201 and replace 50 Ω Termination.

20. Set Dual Pulse Generator (still connected to Oscilloscope) for positive pulse and connect to TP23004 on S-1403C Modulator Assembly.

21. Disconnect Heterodyne Monitor RF IN from RF I/O Connector (9).

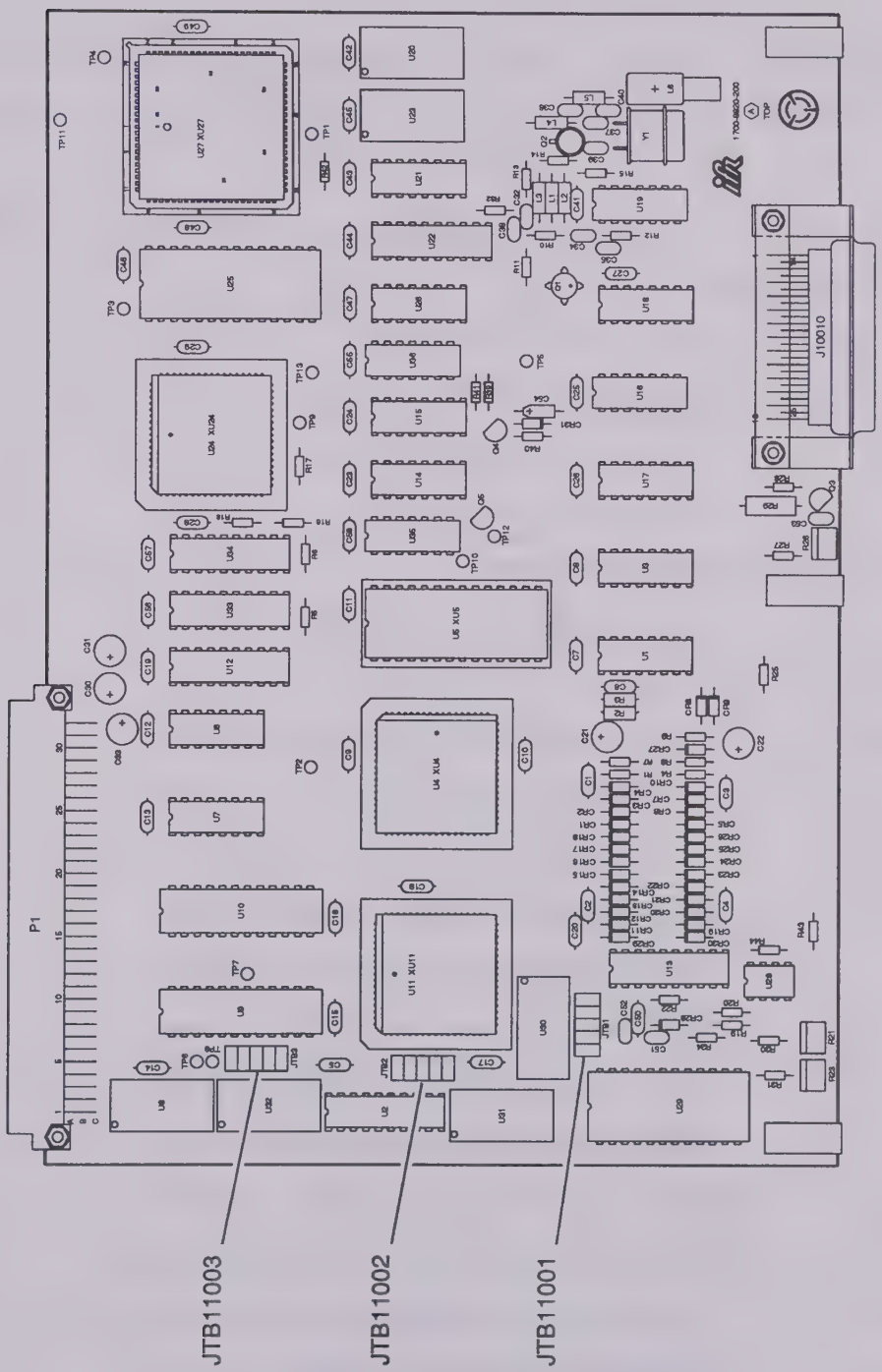
22. Remove AT31001 termination and connect Heterodyne Monitor RF IN to TP31003 on Modulator Assembly. If MLD option is installed, connect 10 dB Attenuator between Heterodyne Monitor and the S-1403C.

23. Use Oscilloscope Δtime to measure delay time between $P_3$ and $F_1$.

24. Verify ***RpDly:*** field value equals Δtime reading (±100 ns). If not, adjust R12005 (ANT B REPLY DELAY Adjust [S]).

25. Remove power and disconnect test equipment.

26. Reconnect AT31001 termination to TP31003.




8807008

Pulse PC Board Assembly Jumper Terminal Blocks
Figure 30

G. Calibration/Verification Data Sheet

TECHNICIAN: _____ DATE: _____

ATC-1400A S/N: _____ S-1403C S/N: _____

| STEP | DATA | RESULT |
|---|---|---|
| (1) | Power Supply | |
| 3. | +5 Vdc (+4.95 to +5.05 Vdc) | _____ |
| 5. | +12 Vdc (+11.95 to +12.05 Vdc) | _____ |
| 7. | -12 Vdc (-12.25 to -11.75 Vdc) | _____ |
| 9. | +40 Vdc (+35.0 to +45.0 Vdc) | _____ |
| (2) | Interrogation Pulses and SPR | |
| 9. | $P_1$ Rise Time 70 ns (50 to 90 ns) | _____ |
| | $P_1$ Fall Time 70 ns (50 to 90 ns) | _____ |
| 11. | $P_1$ Pulse Width 0.80 µs (0.79 to 0.81 µs) | _____ |
| 13. | $P_1$ VAR Width (MIN) 0.20 µs (0.19 to 0.21 µs) | _____ |
| 14. | $P_1$ VAR Width (MAX) 1.85 µs (1.84 to 1.86 µs) | _____ |
| 16. | Mode 1 Spacing 3.00 µs (2.99 to 3.01 µs) | _____ |
| | Mode 2 Spacing 5.00 µs (4.99 to 5.01 µs) | _____ |
| | Mode T Spacing 6.50 µs (6.49 to 6.51 µs) | _____ |
| | Mode 3/A Spacing 8.00 µs (7.99 to 8.01 µs) | _____ |
| | Mode B Spacing 17.00 µs (16.99 to 17.01 µs) | _____ |
| | Mode C Spacing 21.00 µs (20.99 to 21.01 µs) | _____ |
| | Mode D Spacing 25.00 µs (24.99 to 25.01 µs) | _____ |
| 18. | ATC (A) $P_3$ Pulse Width 0.80 µs (0.79 to 0.81 µs) | _____ |
| 19. | ACS (A) $P_1$ to $P_3$ Pulse Spacing 8.00 µs (7.99 to 8.01 µs) | _____ |
| 20. | ACS (A) $P_1$ to $P_4$ Pulse Spacing 10.00 µs (9.99 to 10.01 µs) | _____ |

| STEP | DATA | RESULT |
|---|---|---|
| 21. | ACS (A) $P_4$ Pulse Width 0.80 µs (0.79 to 0.81 µs) | _____ |
| 23. | ACS (A) $P_4$ Pulse Width (MIN)<br>200 ns (190 to 210 ns) | _____ |
| | ACS (A) $P_4$ Pulse Width (MAX)<br>2.75 µs (2.74 to 2.76 µs) | _____ |
| 25. | ACL (A) $P_1$ to $P_3$ Pulse Spacing<br>8.00 µs (7.99 to 8.01 µs) | _____ |
| 26. | ACL (A) $P_1$ to $P_4$ Pulse Spacing<br>10.00 µs (9.99 to 10.01 µs) | _____ |
| 27. | ACL (A) $P_4$ Pulse Width 1.60 µs (1.59 to 1.61 µs) | _____ |
| 29. | ACL (A) $P_4$ Pulse Width (MIN)<br>200 ns (190 to 210 ns) | _____ |
| | ACL (A) $P_4$ Pulse Width (MAX)<br>3.55 µs (3.54 to 3.56 µs) | _____ |
| 31. | ACL (C) $P_1$ to $P_3$ Pulse Spacing<br>21.00 µs (20.99 to 21.01 µs) | _____ |
| 32. | ACL (C) $P_1$ to $P_4$ Pulse Spacing<br>23.00 µs (22.99 to 23.01 µs) | _____ |
| 33. | ACS (C) $P_1$ to $P_3$ Pulse Spacing<br>21.00 µs (20.99 to 21.01 µs) | _____ |
| 34. | ACS (C) $P_1$ to $P_4$ Pulse Spacing<br>23.00 µs (22.99 to 23.01 µs) | _____ |
| 37. | ATC (C) $P_1$ to $P_3$ Pulse Spacing (+Δ)<br>22.85 µs (22.84 to 22.86 µs) | _____ |
| 38. | ATC (C) $P_1$ to $P_3$ Spacing (-Δ)<br>19.15 µs (19.14 to 19.16 µs) | _____ |
| 42. | $P_2$ Pulse Amplitude +5 dB (4.5 to 5.5 dB) | _____ |
| 46. | $P_3$ Pulse Amplitude -19 dB (-19.5 to -18.5 dB) | _____ |
| 48. | $P_3$ Pulse Amplitude -10 dB (-10.3 to -9.7 dB) | _____ |
| 50. | $P_3$ Pulse Amplitude 6 dB (5.5 to 6.5 dB) | _____ |
| 52. | $P_3$ Pulse Amplitude 0 dB (-0.3 to +0.3 dB) | _____ |
| 60. | $P_6$ even Pulse Amplitude | _____ (√) |

| STEP | DATA | RESULT |
|---|---|---|
| 61. | SEQ $P_6$ (UF16) Pulse Width<br>30.25 µs (30.24 to 30.26 µs) | _____ |
| 62. | SEQ $P_6$ (UF00) Pulse Width<br>16.25 µs (16.24 to 16.26 µs) | _____ |
| 64. | SEQ $P_1$ to $P_6$ Pulse Spacing<br>3.50 µs (3.49 to 3.51 µs) | _____ |
| 67. | SEQ $P_6$ Pulse Width (MIN)<br>14.75 µs (14.74 to 14.76 µs) | _____ |
| | SEQ $P_6$ Pulse Width (MAX)<br>17.75 µs (17.74 to 17.76 µs) | _____ |
| 68. | SEQ $P_1$ to $P_2$ Pulse Spacing<br>2.00 µs (1.99 to 2.01 µs) | _____ |
| 69. | SEQ $P_2$ Pulse Width 800 ns (790 to 810 ns) | _____ |
| 71. | SEQ $P_1$ to $P_2$ Pulse Spacing (+Δ)<br>3.85 µs (3.84 to 3.86 µs) | _____ |
| 72. | SEQ $P_1$ to $P_2$ Pulse Spacing (-Δ)<br>150 ns (140 to 160 ns) | _____ |
| 75. | $P_2$ to SPR Pulse Spacing<br>2.75 µs (2.74 to 2.76 µs) | _____ |
| 76. | SPR and $P_6$ Transition Times <80 ns | _____(√) |
| 78. | $P_2$ to SPR Pulse Spacing (MIN)<br>1.75 µs (1.74 to 1.76 µs) | _____ |
| | $P_2$ to SPR VAR Pulse Spacing (MAX)<br>3.75 µs (3.74 to 3.76 µs) | _____ |
| 85. | $P_5$ Leading Edge Position to SPR<br>400 ns (300 to 500 ns) | _____ |
| 89. | SPR to $P_5$ Trailing Edge Position<br>400 ns (300 to 500 ns) | _____ |
| 90. | $P_5$ Pulse Width 800 ns (700 to 900 ns) | _____ |
| (3) | Suppressor and Interference Pulses | |
| 10. | Interference to $P_1$ Pulse Spacing<br>17.5 µs (17.4491 to 17.5509 µs) | _____ |
| 11. | Interference to $P_1$ Pulse Spacing<br>399 µs (398.93 to 399.07 µs) | _____ |

| STEP | | DATA | RESULT |
|---|---|---|---|
| | 12. | Interference Pulse Width (MIN) 200 ns | _____ (√) |
| | | Interference Pulse Width (MAX) 5.0 µs | _____ (√) |
| | 14. | DI First Pulse to $P_1$ Pulse Spacing 200 µs (199.95 to 200.05 µs) | _____ |
| | 15. | First Interrogation Removed | _____ (√) |
| | 18. | ATC Suppression Pulse to $P_3$ Pulse Spacing 800 ns (700 to 900 ns) | _____ |
| | 19. | SEQ Suppression Pulse to SPR Pulse Spacing 800 ns (700 to 900 ns) | _____ |
| | 20. | ACS Suppression Pulse to $P_3$ Pulse Spacing 800 ns (700 to 900 ns) | _____ |
| | 21. | ACL Suppression Pulse to $P_3$ Pulse Spacing 800 ns (700 to 900 ns) | _____ |
| (4) | RF Level | | |
| | 5. | ATC-1400A (Antenna A) Power Meter reference reading (RF output to ATC-1400A disconnected) | _____ |
| | 6. | Antenna A Power Meter reading does not change (RF output to ATC-1400A connected) <0.05 dB difference | _____ (√) |
| | 7. | Antenna A RF Level Change (MAX) +3.0 dB (+2.7 to +3.3 dB) | _____ |
| | 8. | Antenna A RF Level Change (MIN) -3.0 dB (-3.3 to -2.7 dB) | _____ |
| | 9. | Antenna A Level Change 0 dB (-0.05 to +0.05 dB) | _____ |
| | 15. | Antenna A Signal Level reference | _____ |
| | 17. | Antenna B Signal Level Step 15 reference (±1 dB) | _____ |
| | 22. | Antenna B (with MLD option) Power Meter reference reading -20 dBm (-21 to -19 dBm) | _____ |
| | 23. | Antenna B (with MLD option) RF Level Change (MAX) +3.0 dB (+2.7 to +3.3 dB) | _____ |
| | 24. | Antenna B (with MLD option) RF Level Change (MIN) -3.0 dB (-3.3 to -2.7 dB) | _____ |

| STEP | DATA | RESULT |
|---|---|---|
| (5) Antenna B | | |
| 12. | Sync to $P_1$ Pulse Spacing reference (Antenna A, ATC-1400A) | _____ |
| 21. | $P_1$ (Antenna B, -3.0 dB setting) aligned with major vertical ($P_1$ [Antenna B, +3.0 dB setting]) | _____(√) |
| 24. | $P_1$ (Antenna B, +3.0 dB setting) aligned with major vertical ($P_1$ [Antenna B, -3.0 dB setting]) | _____(√) |
| 28. | $P_1$ (Antenna B, S-1403C) conincident with $P_1$ (Antenna A) 0 ns (-25 to +25 ns) | _____ |
| 29. | $P_1$ (Antenna B) Pulse Width 800 ns (790 to 810 ns) | _____ |
| 30. | $P_2$ to SPR (Antenna B) Spacing 2.75 µs (2.70 to 2.80 µs) | _____ |
| 31. | SPR to second Phase Transition (Antenna B) 1.0 µs (990 to 1010 ns) | _____ |
| 33. | $P_1$ (Antenna B) positive position shift 950 ns (900 to 1000 ns) | _____ |
| 34. | $P_1$ (Antenna B) negative position shift -950 ns (-1000 to -900 ns) | _____ |
| 38. | Antenna B Frequency 1030.00 MHz (1029.99 to 1030.01 MHz) | _____ |
| 39. | TCXO input Voltage 6.0 Vdc (5.5 to 6.5 Vdc) | _____ |
| 40. | TCXO course adjust 1030 MHz (1029.9996 to 1030.0004) | _____ |
| 41. | R16003 (TCXO) fine adjust 1030 MHz (1029.999950 to 1030.000050 MHz) | _____ |
| (6) Reply Delay and PPMG | | |
| 11. | Power Display reference reading | _____ |
| 12. | $P_3$ to $F_1$ Pulse Spacing (Reply Delay) | _____ |
| 13. | Antenna A Reply Delay Reading (Reply Delay ±100 ns) | _____ |
| 14. | Power Display reading not changed | _____(√) |
| 16. | PPG, Power Display reading changed <10% | _____(√) |

| STEP | DATA | RESULT |
|---|---|---|
| 18. | PPG, SPI, Power Display reads 0 | _____ (√) |
| 23. | Reply Delay Time from $P_3$ to $F_1$ | _____ |
| 24. | Antenna B Reply Delay Reading (Reply Delay ±100 ns) | _____ |

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## 3. PC Boards and Schematics

### A. General

This section contains component layout drawings for all PC Board Assemblies, Interconnect Diagrams and Circuit Schematics within the S-1403C with or without MLD installed.

### B. How To Use Schematics

To trace coaxial cable conductors from one schematic to another, follow the procedure outlined in 2-2-3B(1) To trace conductors for multiple pin connectors, follow the procedure outlined in 2-2-3B(2).

(1) Coaxial Cables

| STEP | PROCEDURE |
|---|---|

1. Locate desired assembly or module on Interconnect Diagram.
2. Locate desired coaxial cable on Interconnect Diagram.

   **NOTE:** Connectors are identified by reference designators.

3. Follow coaxial cable on Interconnect Diagram to locate opposite end of conductor. Note coaxial cable reference designator and destination.
4. Locate schematic of desired assembly or module in 2-2-3C.
5. Locate reference designator of coaxial cable and continue tracing circuit.

(2) Multiple Pin Connectors

| STEP | PROCEDURE |
|---|---|

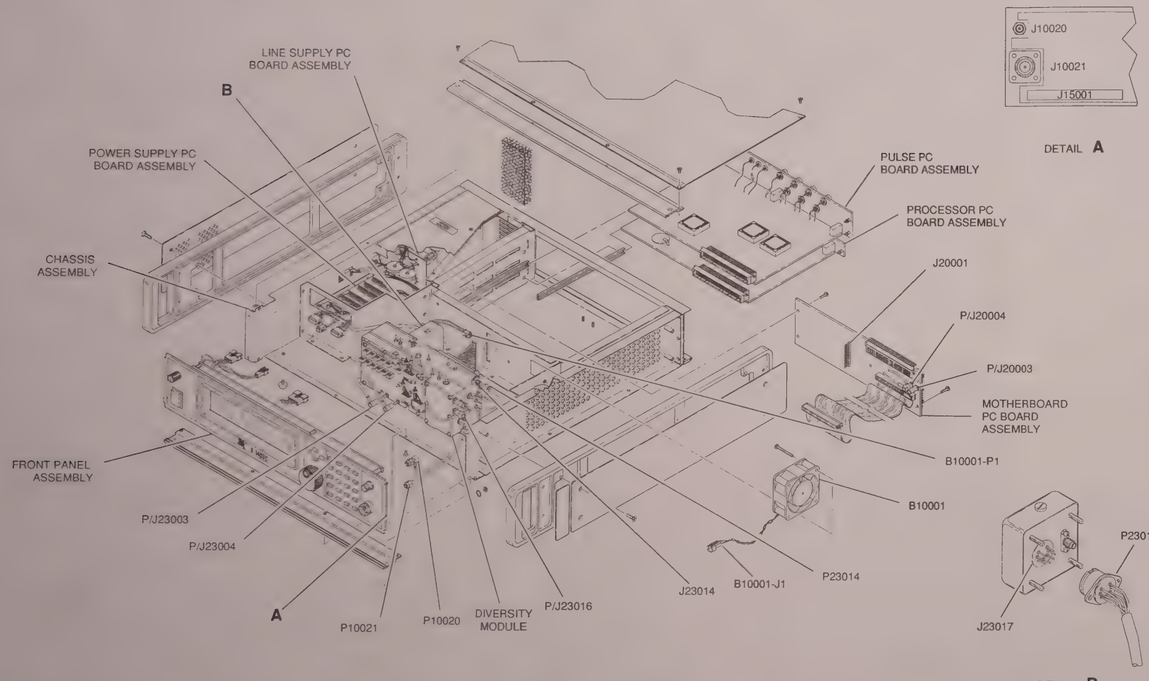
1. Locate desired assembly or module on Interconnect Diagram.
2. Locate desired multiple pin connector on Interconnect Diagram.

   **NOTE:** Connectors are identified by reference designators.

3. Note reference designator of the mating connector. Note assembly, module or wire harness, connector is mounted on or grouped with.
4. Locate schematic of desired assembly or module in 2-2-3C.
5. Locate reference designator of multiple pin connector and corresponding pin number. Continue tracing circuit.

C. Alphabetical Index of Assemblies, Interconnect Diagrams and Circuit Schematics

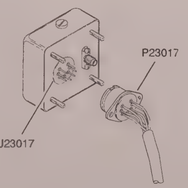

| TITLE | PAGE |
|---|---|
| 1030 MHz Source PC Board Assembly | 22 |
| Attenuator Assembly | 28 |
| Attenuator Assembly Circuit Schematic | 28 |
| Attenuator Driver PC Board Assembly | 28 |
| Composite Assembly (w/ MLD) | 4 |
| Composite Assembly (w/o MLD) | 3 |
| Composite Assembly (w/ MLD) Interconnect Diagram | 4 |
| Composite Assembly (w/o MLD) Interconnect Diagram | 3 |
| Diversity I/O PC Board Assembly | 24 |
| Diversity Module (w/ MLD) | 20 |
| Diversity Module (w/o MLD) | 19 |
| Diversity Module (w/ MLD) Interconnect Diagram | 20 |
| Diversity Module (w/o MLD) Interconnect Diagram | 19 |
| Front Panel Assembly | 10 |
| Front Panel Assembly Interconnect Diagram | 10 |
| Front Panel Processor PC Board Assembly (w/ MLD) | 14 |
| Front Panel Processor PC Board Assembly (w/o MLD) | 12 |
| Front Panel Processor PC Board Assembly (w/ MLD) Circuit Schematic | 15 |
| Front Panel Processor PC Board Assembly (w/o MLD) Circuit Schematic | 13 |
| Inverter Supply PC Board Assembly | 6 |
| Keyboard PC Board Assembly | 11 |
| Keyboard PC Board Assembly Circuit Schematic | 11 |
| Line Supply PC Board Assembly | 5 |
| Line Supply PC Board Assembly Circuit Schematic | 5 |
| Modulator Assembly (w/ MLD) | 26 |
| Modulator Assembly (w/o MLD) | 24 |
| Modulator Assembly (w/ MLD) Circuit Schematic | 27 |
| Modulator Assembly (w/o MLD) Circuit Schematic | 25 |
| Modulator PC Board Assembly (w/ MLD) | 26 |
| Modulator PC Board Assembly (w/o MLD) | 24 |
| Motherboard PC Board Assembly | 18 |
| Motherboard PC Board Assembly Circuit Schematic | 18 |
| Power Amp PC Board Assembly | 22 |
| Power Distribution PC Board Assembly | 6 |
| Power Supply Assembly | 6 |
| Power Supply Assembly Circuit Schematic | 7 |
| Power Termination Assembly | 21 |
| Power Termination Assembly Circuit Schematic | 21 |
| Power Termination PC Board | 21 |
| Processor PC Board Assembly | 8 |
| Processor PC Board Assembly Circuit Schematic | 9 |
| Pulse PC Board Assembly | 16 |
| Pulse PC Board Assembly Circuit Schematic | 17 |
| Source/Pwr Amp Assembly | 22 |
| Source/Pwr Amp Assembly Circuit Schematic | 23 |
| Video Detector PC Board Assembly | 21 |
| Video Detector PC Board Assembly Circuit Schematic | 21 |
| Video Filter PC Board Assembly | 24 |



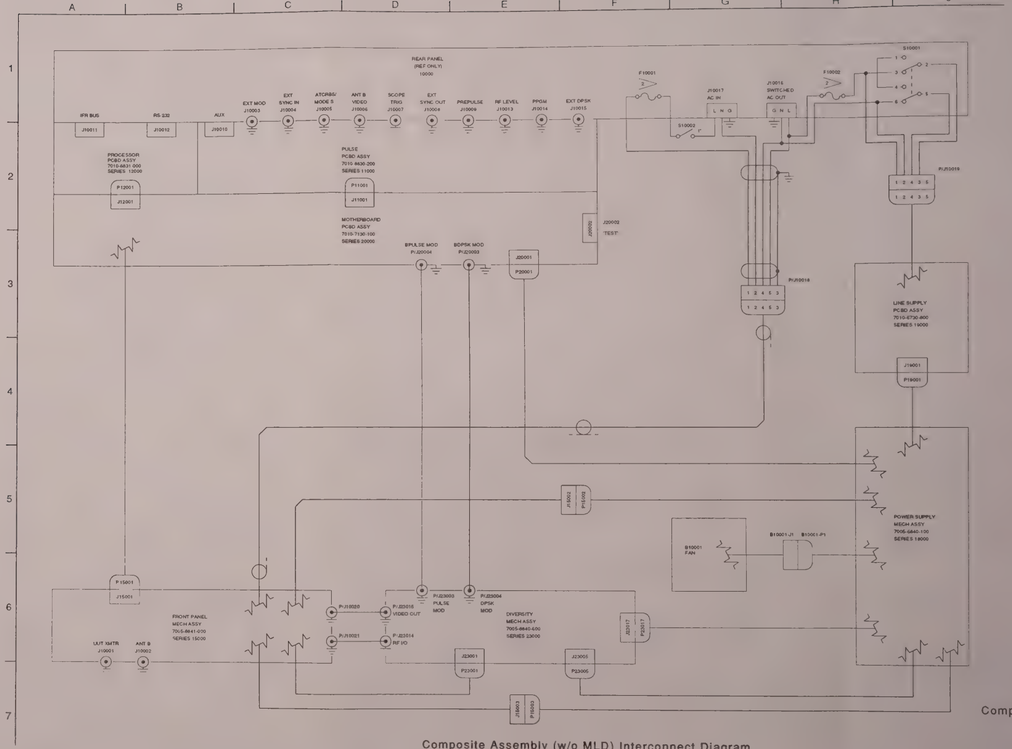

Composite Assembly (w/o MLD)
(7003-8840-000-A1)




DETAIL **A**




DETAIL **B**

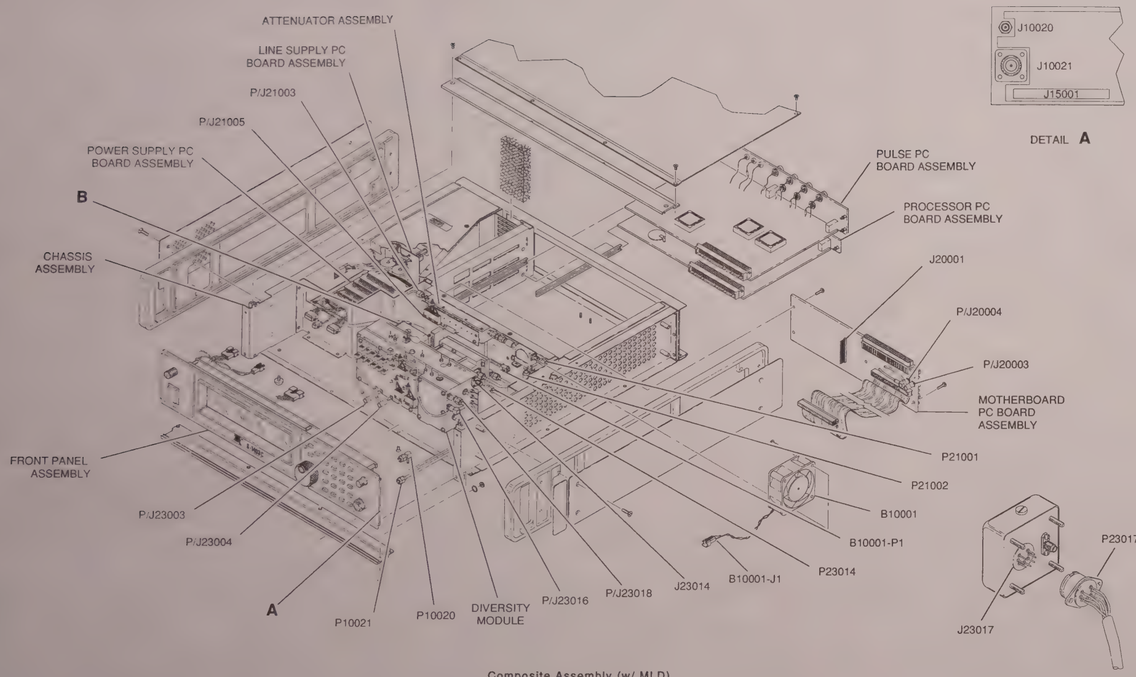



Composite Assembly (w/o MLD) Interconnect Diagram
(0000-8840-000-A1)

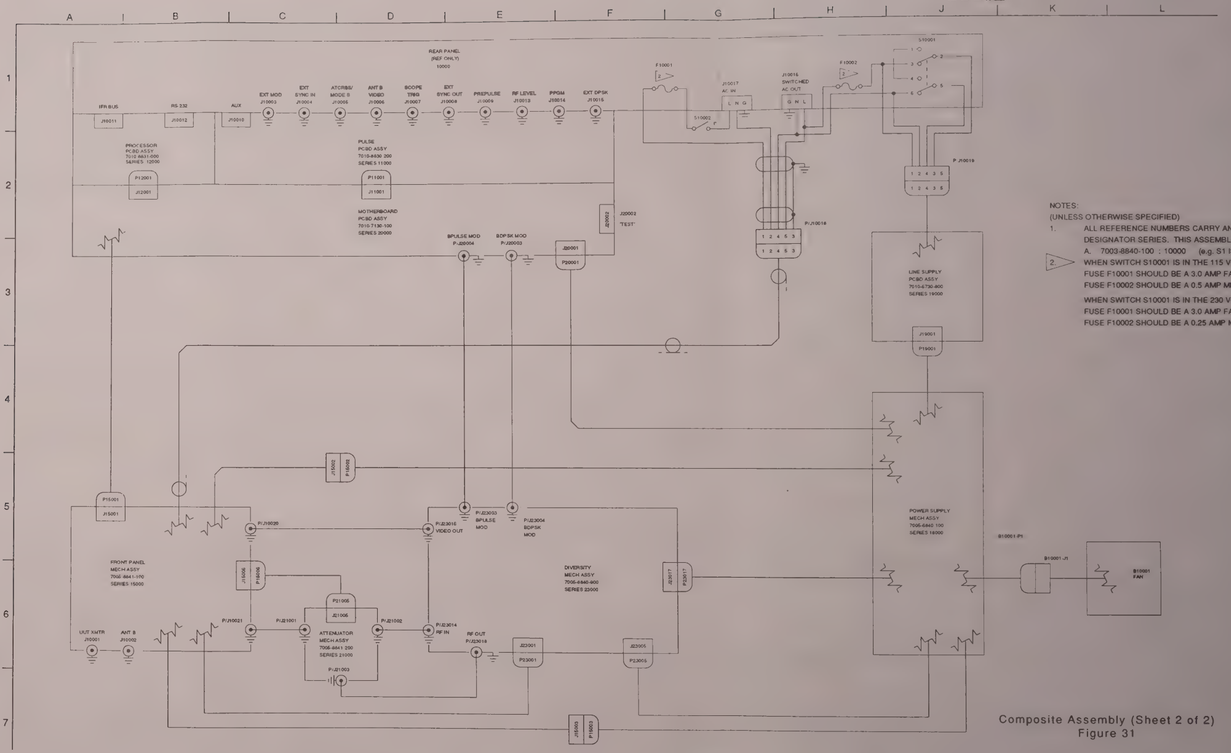
NOTES:
(UNLESS OTHERWISE SPECIFIED)

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7003-8840-000 : 10000 (e.g. S1 IS S10001).
2. WHEN SWITCH S10001 IS IN THE 115 VOLT POSITION:
   FUSE F10001 SHOULD BE A 3.0 AMP FAST-BLOW FUSE.
   FUSE F10002 SHOULD BE A 0.5 AMP MED-BLOW FUSE.
   WHEN SWITCH S10001 IS IN THE 230 VOLT POSITION:
   FUSE F10001 SHOULD BE A 3.0 AMP FAST-BLOW FUSE.
   FUSE F10002 SHOULD BE A 0.25 AMP MED-BLOW FUSE.

Composite Assembly (Sheet 1 of 2)
Figure 31



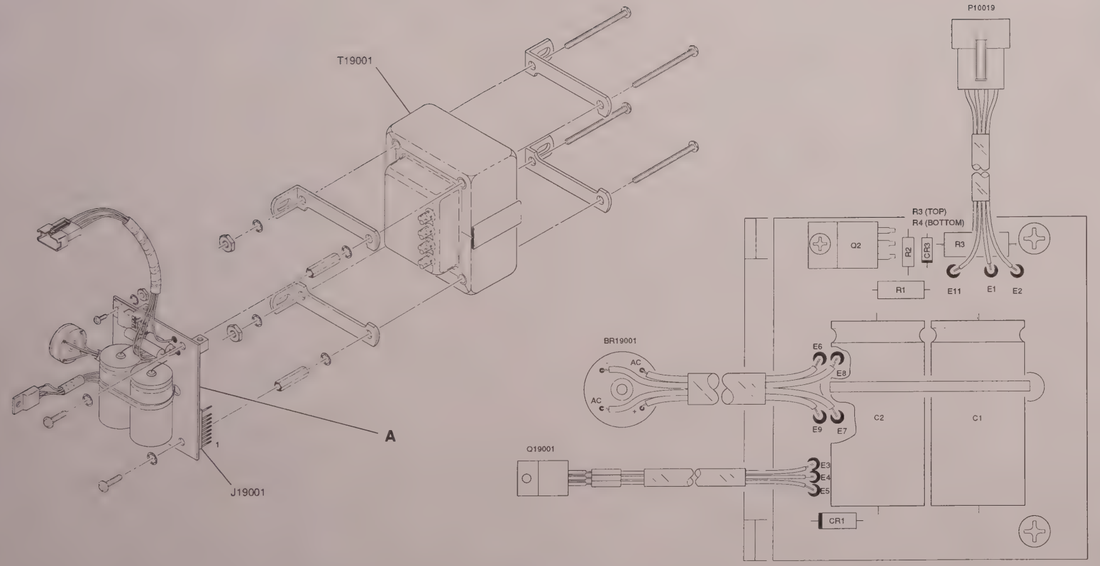

Composite Assembly (w/ MLD)
(7003-8840-100-A1)




NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7003-8840-100 : 10000 (e.g. S1 IS S10001).
2. WHEN SWITCH S10001 IS IN THE 115 VOLT POSITION:
   FUSE F10001 SHOULD BE A 3.0 AMP FAST-BLOW FUSE.
   FUSE F10002 SHOULD BE A 0.5 AMP MED-BLOW FUSE.
   WHEN SWITCH S10001 IS IN THE 230 VOLT POSITION:
   FUSE F10001 SHOULD BE A 3.0 AMP FAST-BLOW FUSE.
   FUSE F10002 SHOULD BE A 0.25 AMP MED-BLOW FUSE.

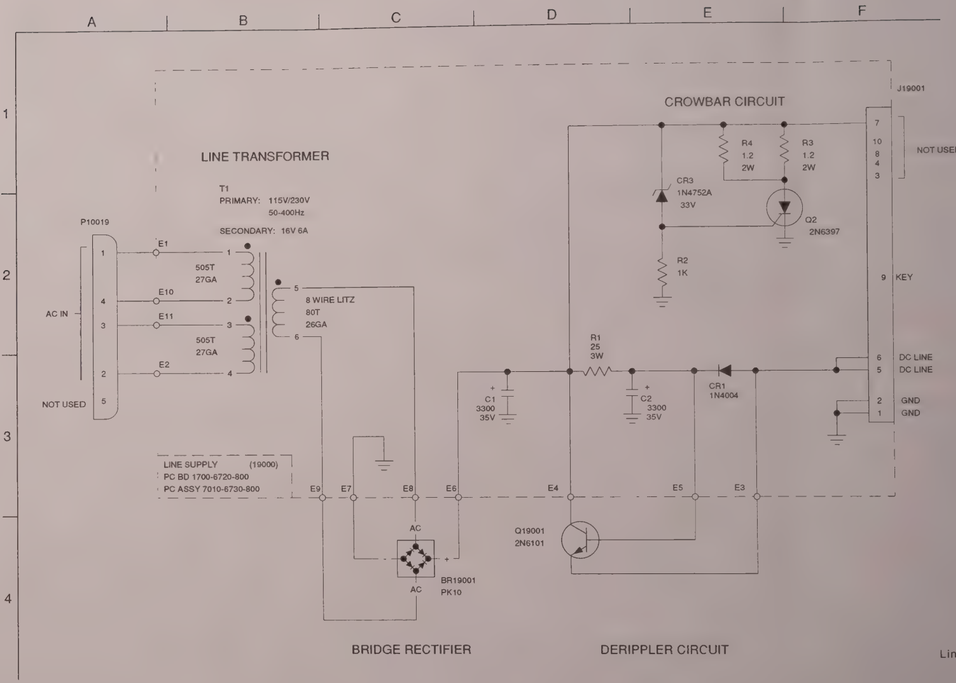
Composite Assembly (Sheet 2 of 2)
Figure 31

Composite Assembly (w/ MLD) Interconnect Diagram
(0000-8840-100-A1)




Line Supply PC Board Assembly
(7010-6730-800-A6)

DETAIL **A**

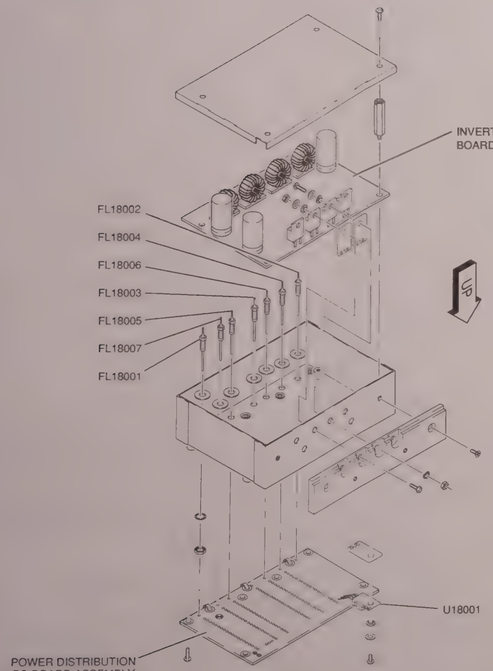



Line Supply PC Board Assembly Circuit Schematic
(7010-6730-800-A6)

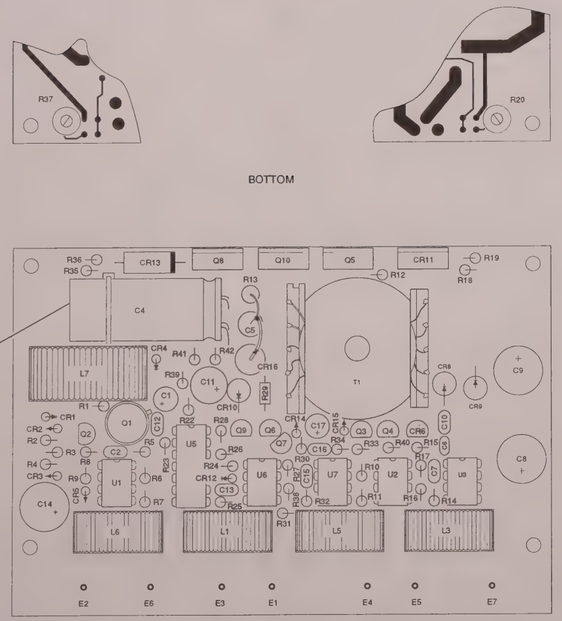
**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES: A. 7010-6730-800 : 19000 (e.g. C1 IS C19001).
2. ALL RESISTORS ARE 1 W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

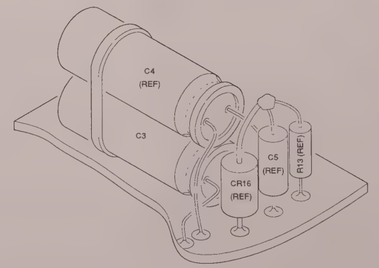
Line Supply PC Board Assembly
Figure 32



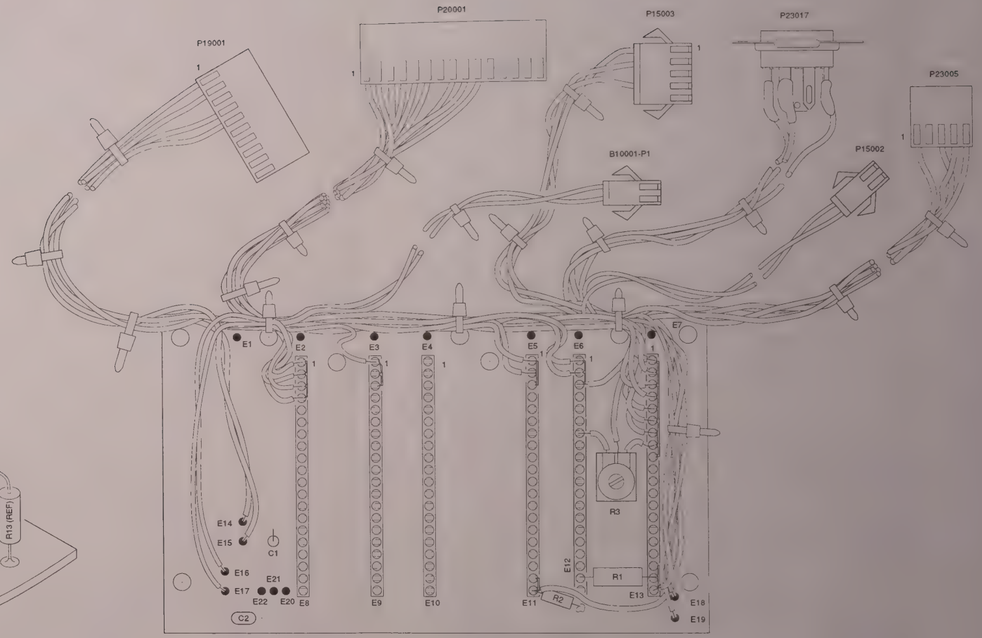

Power Supply Assembly
(7005-6840-100-A2)




Inverter Supply PC Board Assembly
(7010-6730-700-C1)

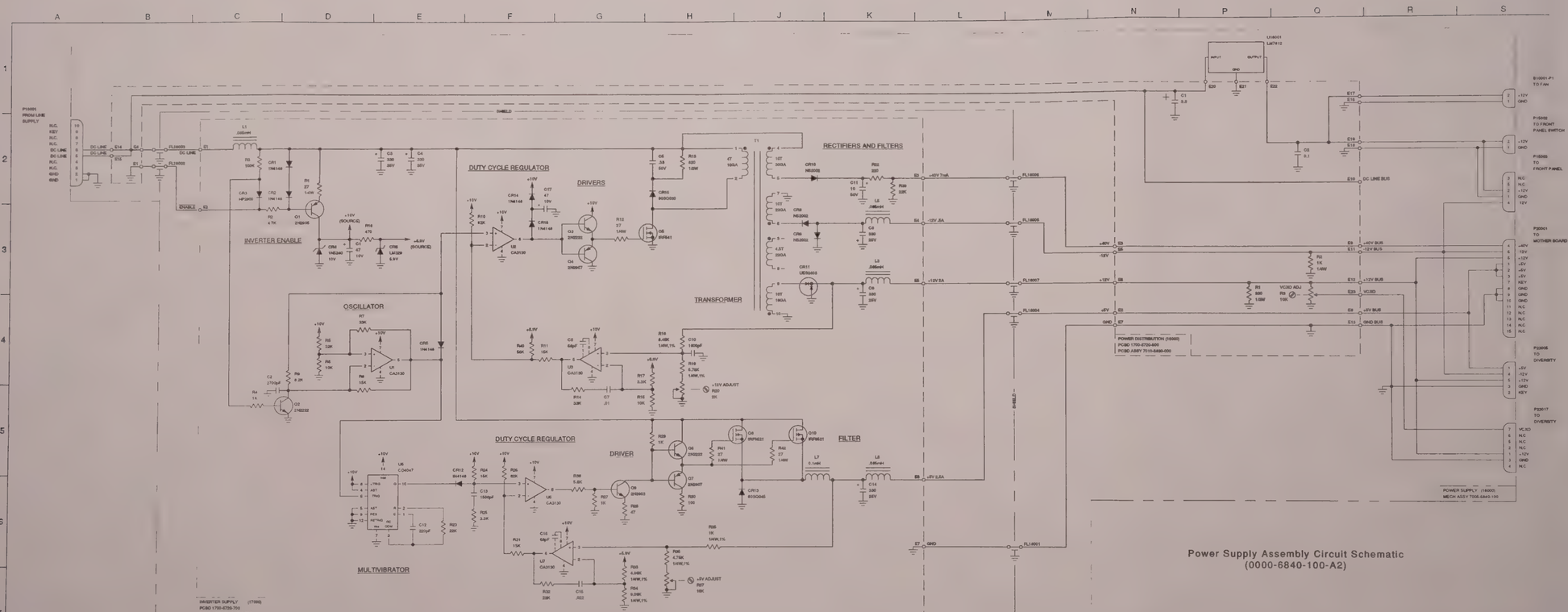



DETAIL **A**




Power Distribution PC Board Assembly
(7010-6830-000-B5)

Power Supply Assembly (Sheet 1 of 2)
Figure 33

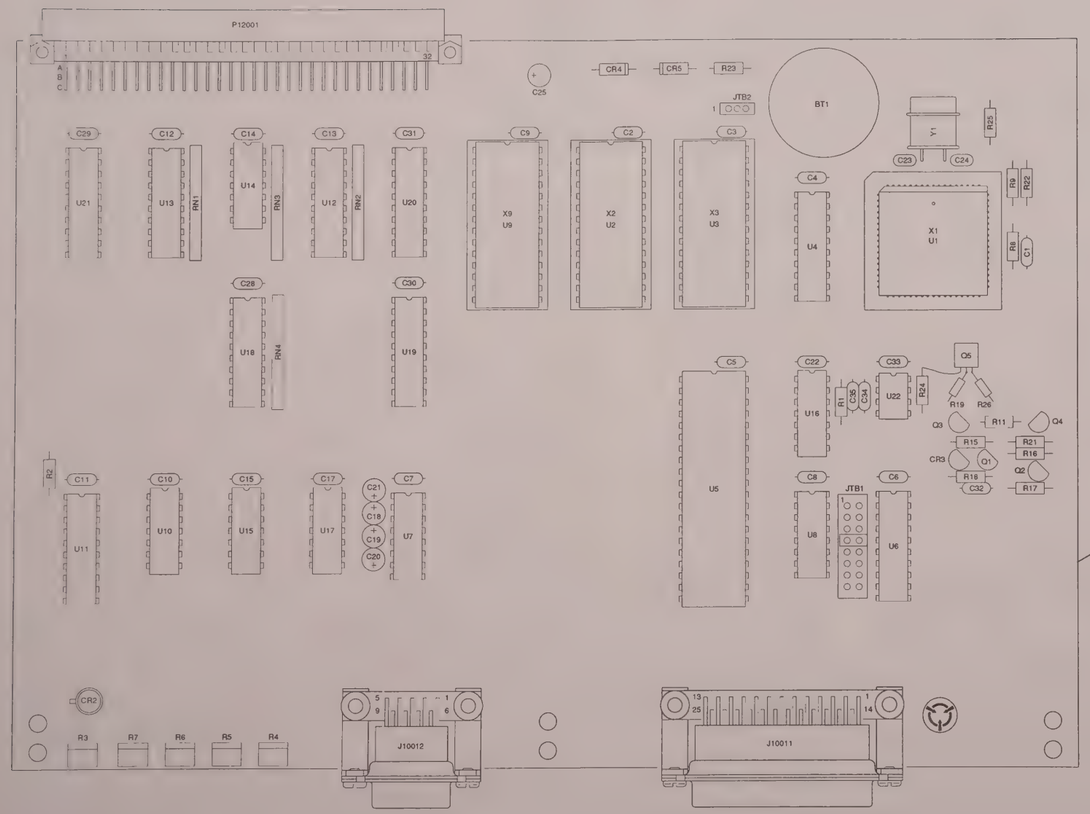



Power Supply Assembly Circuit Schematic
(0000-6840-100-A2)

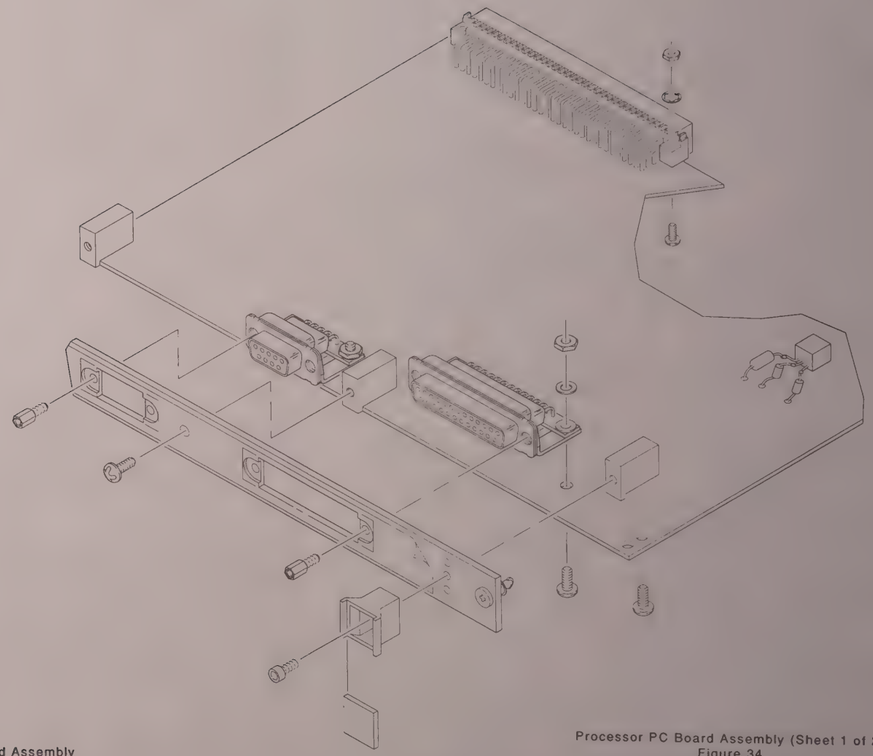
**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7005-6840-100 18000 (e.g. U1 IS U18001)
   B. 7010-6730-700 17000 (e.g. C1 IS C17001)
   C. 7010-6830-000 16000 (e.g. C1 IS C16001).
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

Power Supply Assembly (Sheet 2 of 2)
Figure 33

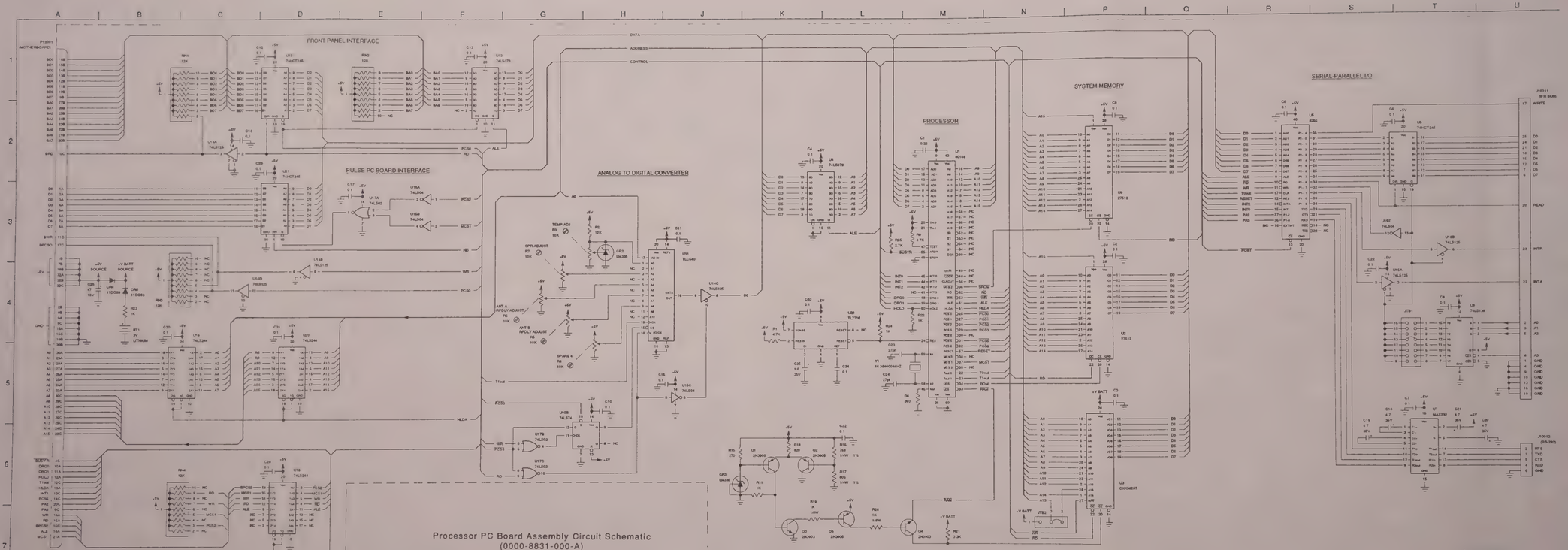



Processor PC Board Assembly
(7010-8831-000-A5)



DETAIL **A**

Processor PC Board Assembly (Sheet 1 of 2)
Figure 34




Processor PC Board Assembly Circuit Schematic
(0000-8831-000-A)

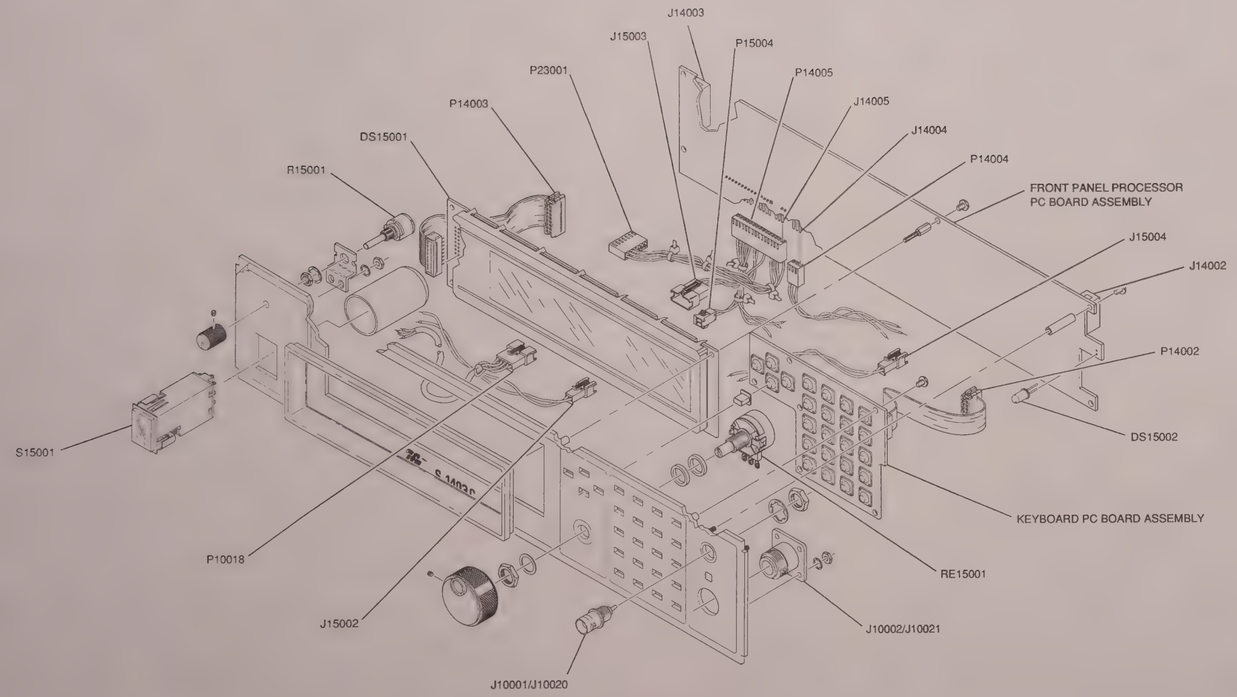
**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

**NOTES:**
(UNLESS OTHERWISE SPECIFIED)

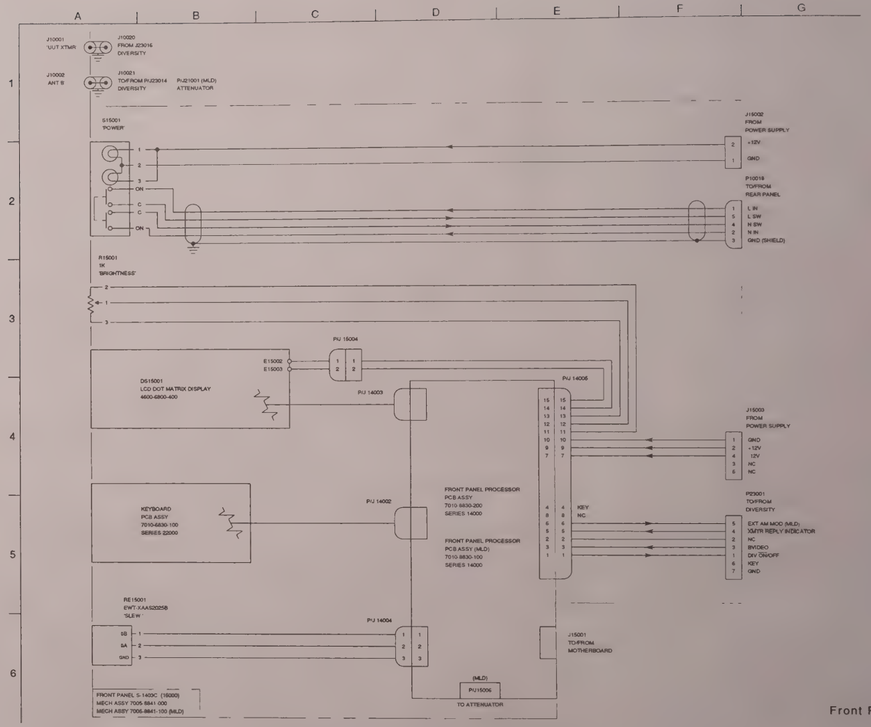
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES: A... 7010-8831-000 :: 12000 (e.g. C1 IS C12001).
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

PROCESSOR (1200)
PCB0: 1760-8821-000
PCBD Au/GT 7010-8831-000

Processor PC Board Assembly (Sheet 2 of 2)
Figure 34




Front Panel Assembly
(7005-8841-000-A1, w/o MLD) (7005-8841-100-A2, w/ MLD)

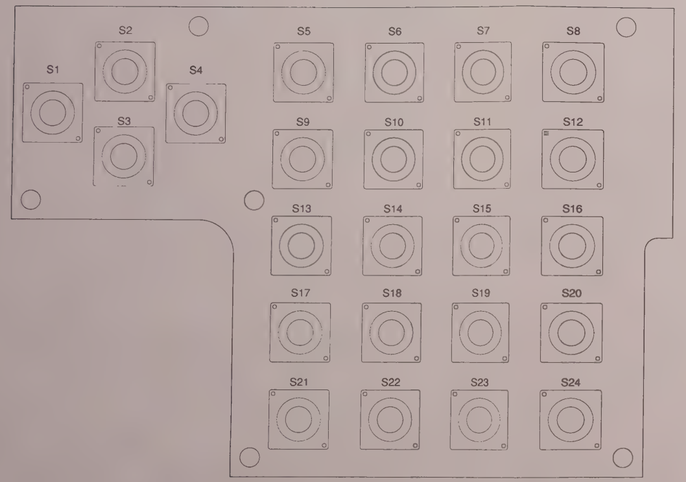



Front Panel Assembly Interconnect Diagram
(0000-8841-000-A, w/o MLD) (0000-8841-100-A, w/ MLD)

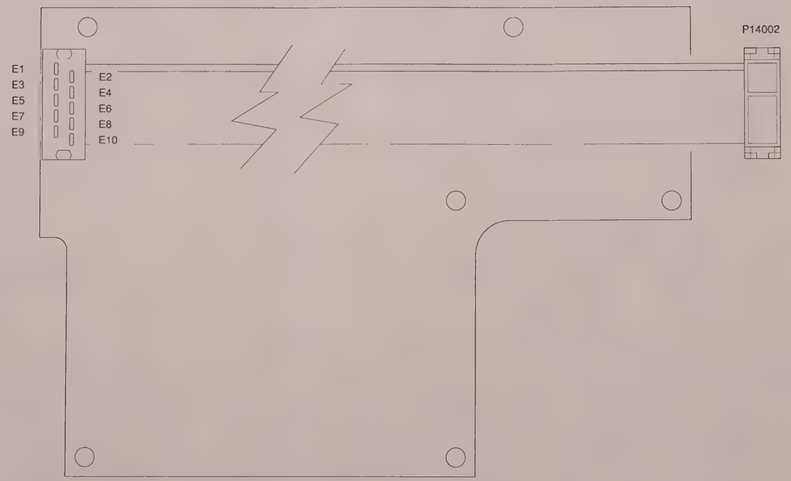
**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7005-8840-000 : 15000 (e.g. R1 IS R15001).
   B. 7005-8840-100 (MLD) : 15000 (e.g. R1 IS R15001).

Front Panel Assembly (Sheet 1 of 6)
Figure 35

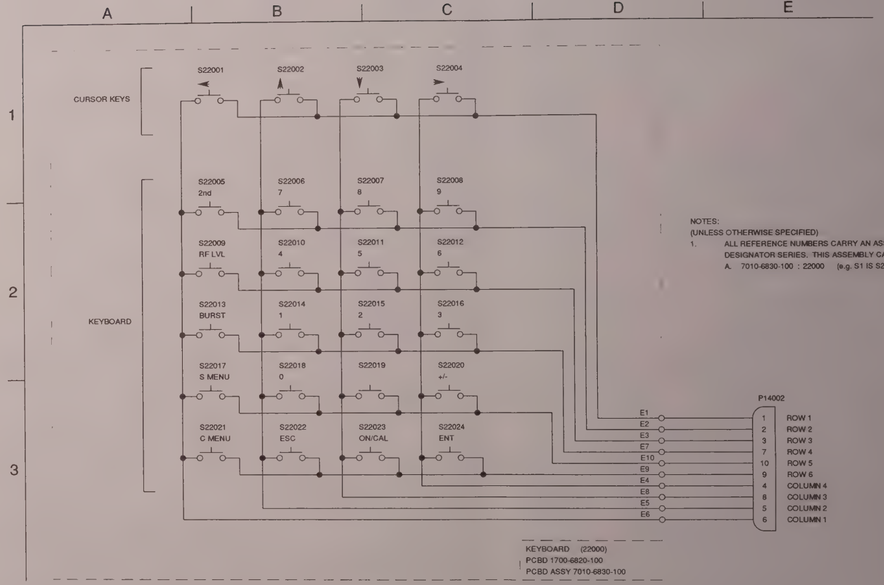



TOP



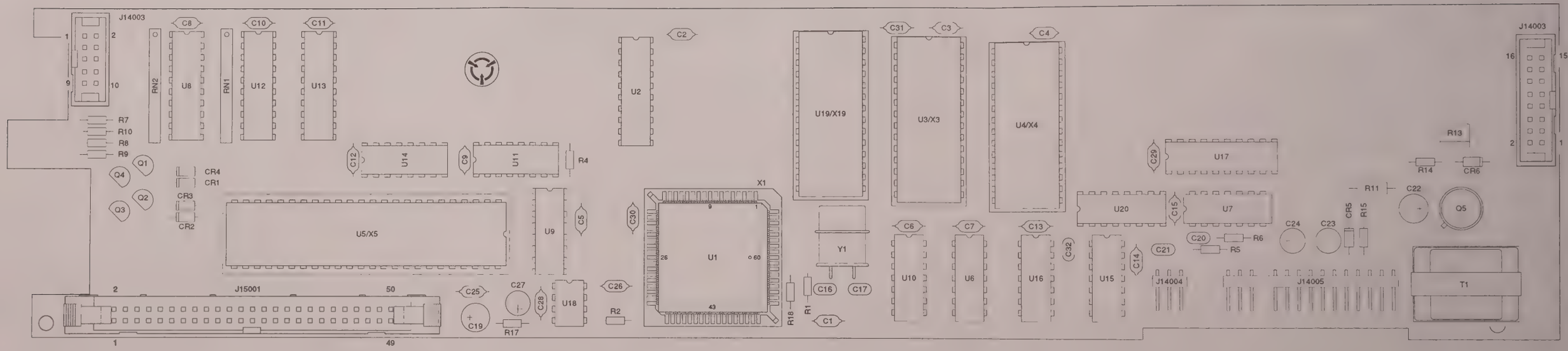

BOTTOM

Keyboard PC Board Assembly
(7010-6830-100-C2)



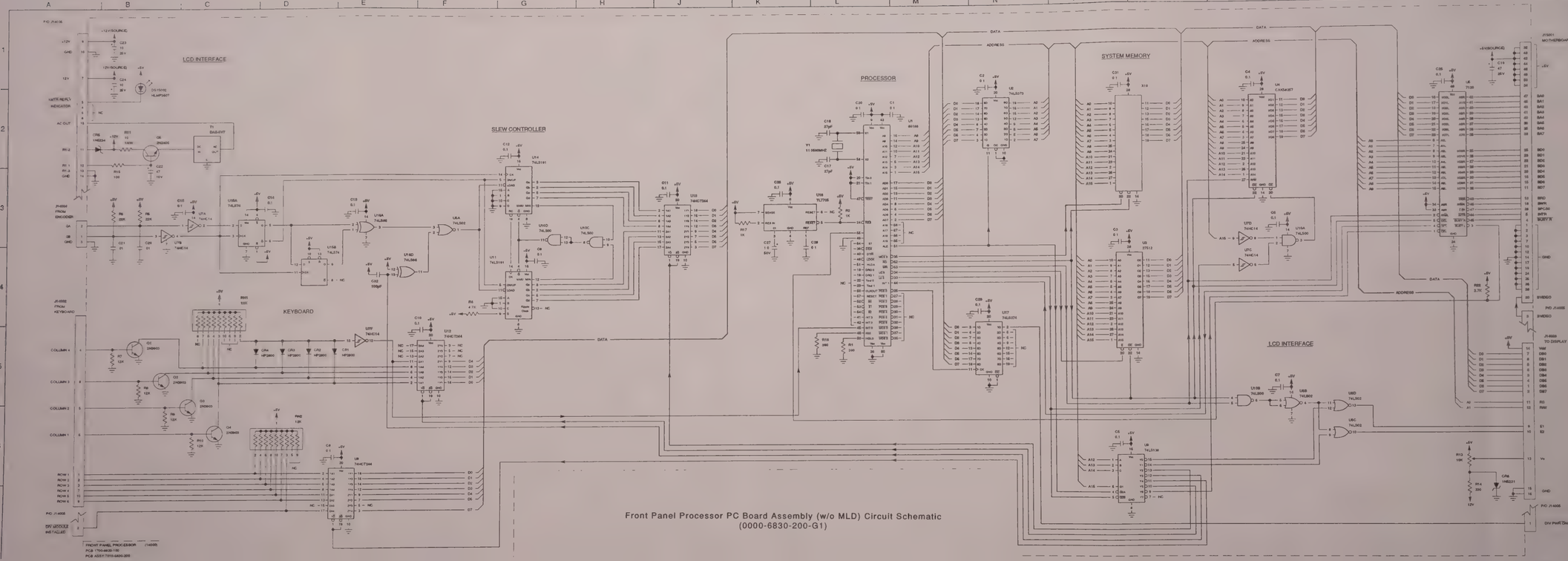

Keyboard PC Board Assembly Circuit Schematic
(0000-6830-100-C1)

Front Panel Assembly (Sheet 2 of 6)
Figure 35




Front Panel Processor PC Board Assembly (w/o MLD)
(7010-6830-200-G1)

Front Panel Assembly (Sheet 3 of 6)
Figure 35

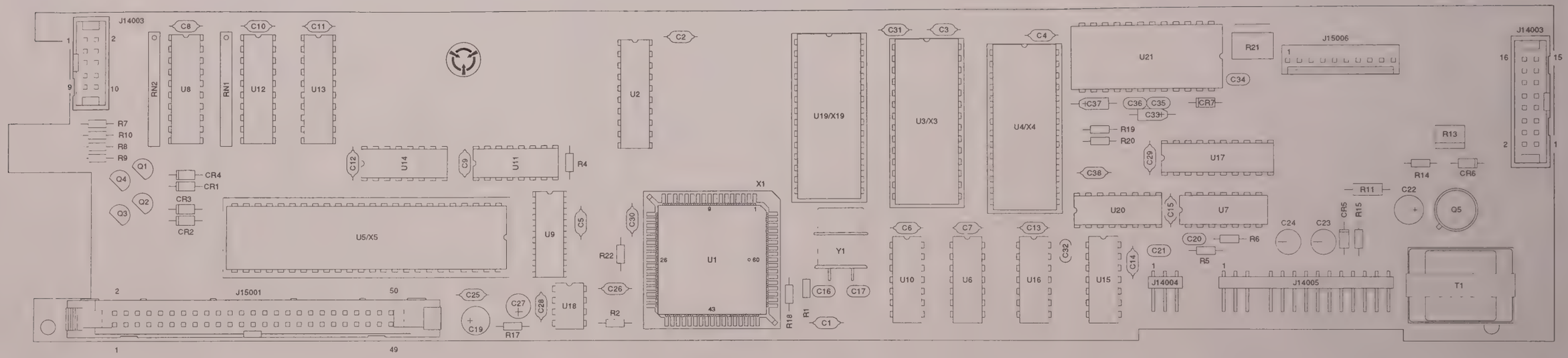



Front Panel Processor PC Board Assembly (w/o MLD) Circuit Schematic
(0000-6830-200-G1)

**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

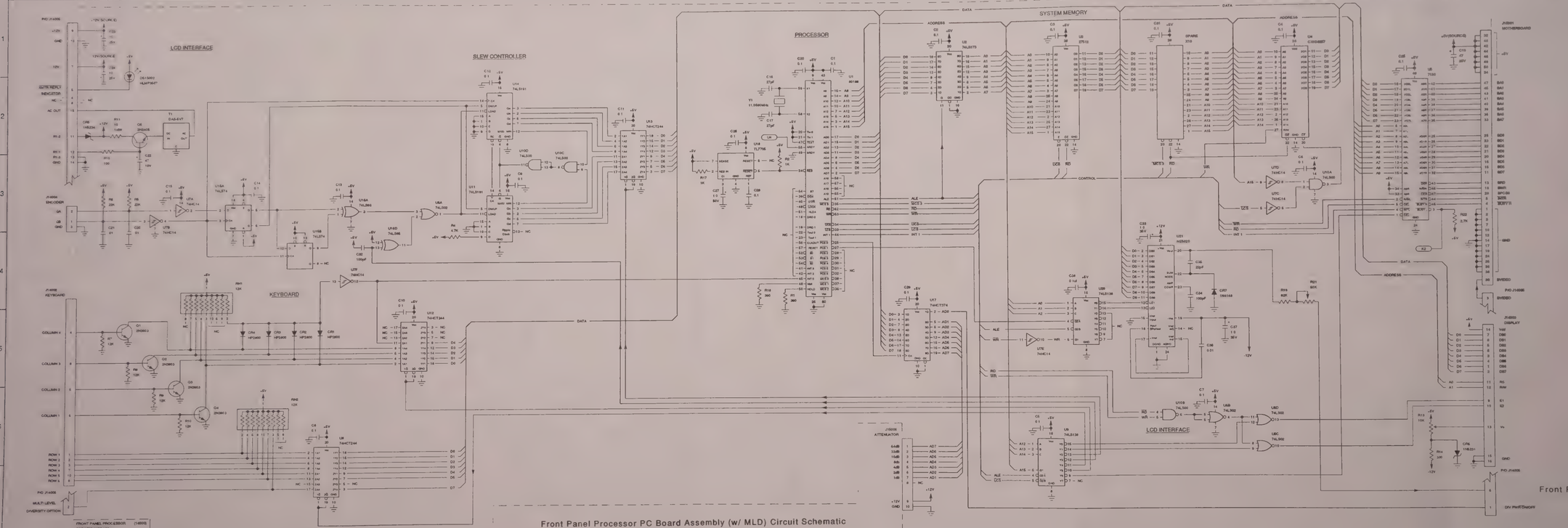
NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A: 7010-6830-200 ; 14000 (e.g. C1 IS C14001).
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

Front Panel Assembly (Sheet 4 of 6)
Figure 35




Front Panel Processor PC Board Assembly (w/ MLD)
(7010-8830-100-A3)

Front Panel Assembly (Sheet 5 of 6)
Figure 35

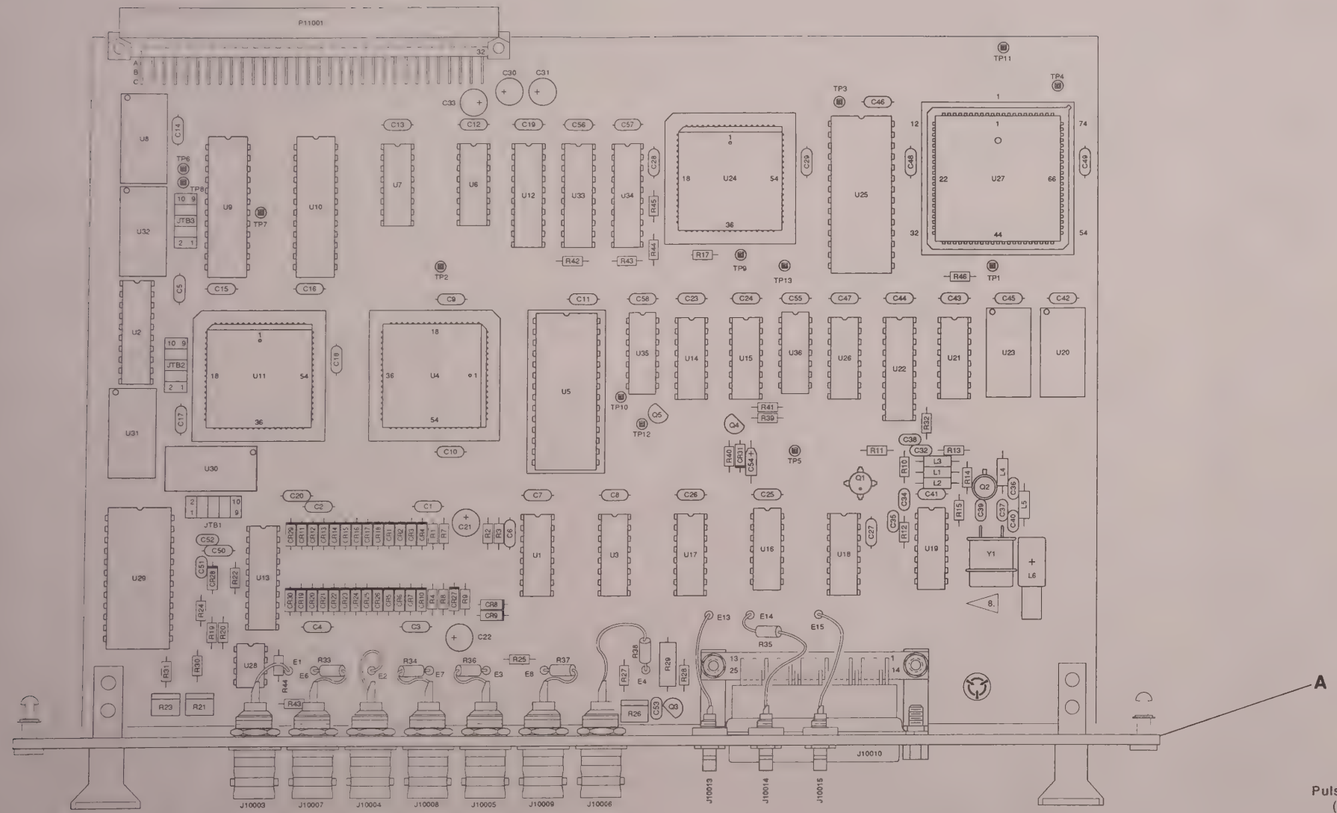



Front Panel Processor PC Board Assembly (w/ MLD) Circuit Schematic
(0000-8830-100-A1)

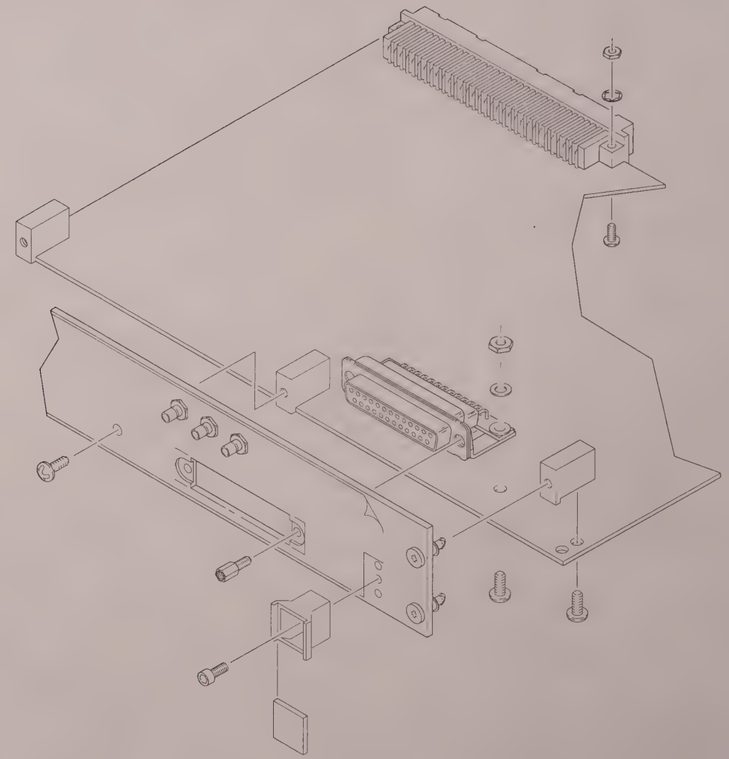
**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A: 7010-8830-100 : 14000 (e.g. C1 IS C14001).
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

Front Panel Assembly (Sheet 6 of 6)
Figure 35




Pulse PC Board Assembly
(7010-8830-200-A5)



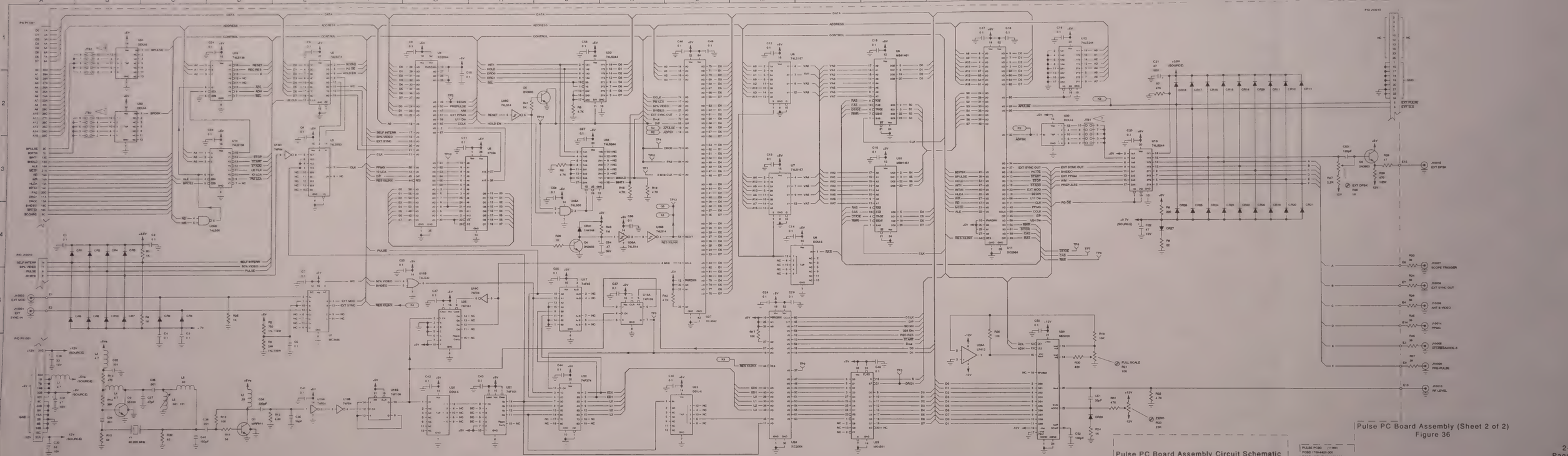
DETAIL **A**

**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7010-8830-300 : 11000 (e.g. C1 IS C11001).
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.
6. ALL DIODES ARE IN4148.
7. JUMPERS ON JUMPER BLOCKS ARE S.A.T.
8. CRYSTAL CASE MUST NOT BE HEATED. DO NOT ALLOW SOLDER TO FLOW OR COME IN CONTACT WITH CRYSTAL CASE.

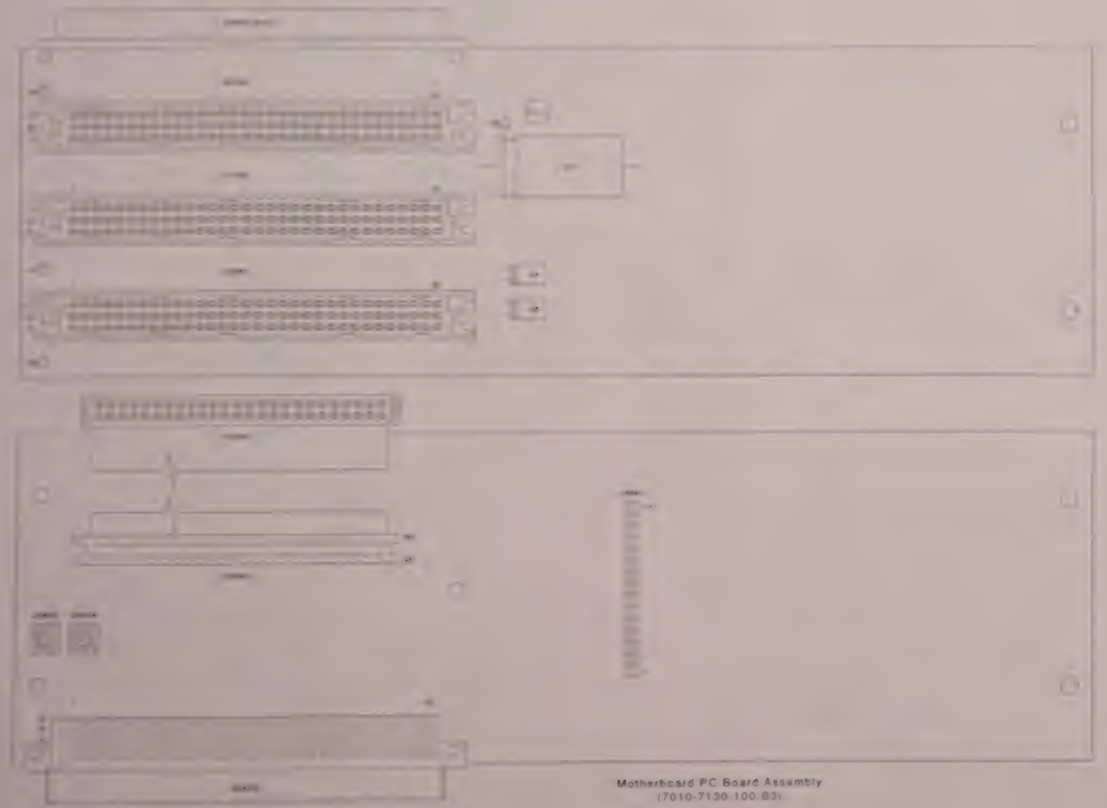
Pulse PC Board Assembly (Sheet 1 of 2)
Figure 36



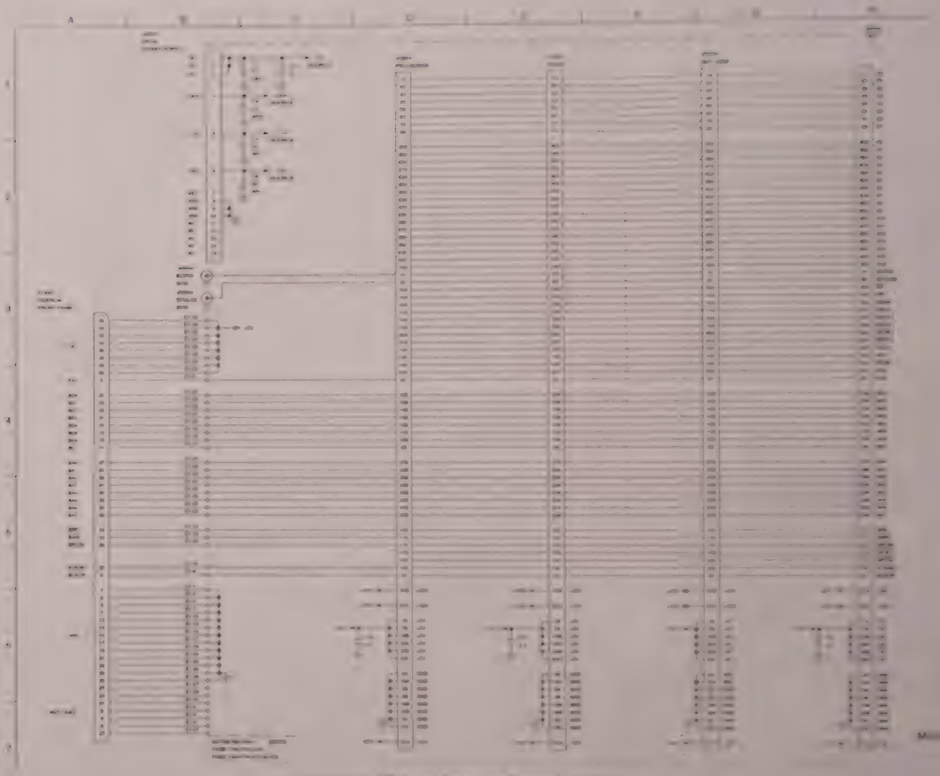
Pulse PC Board Assembly Circuit Schematic
(0000-8830-200-A2)

PULSE PCBC (11166)
PCBD 1760-8401-300
PCBD ASSY 7910-8830-200

Pulse PC Board Assembly (Sheet 2 of 2)
Figure 36



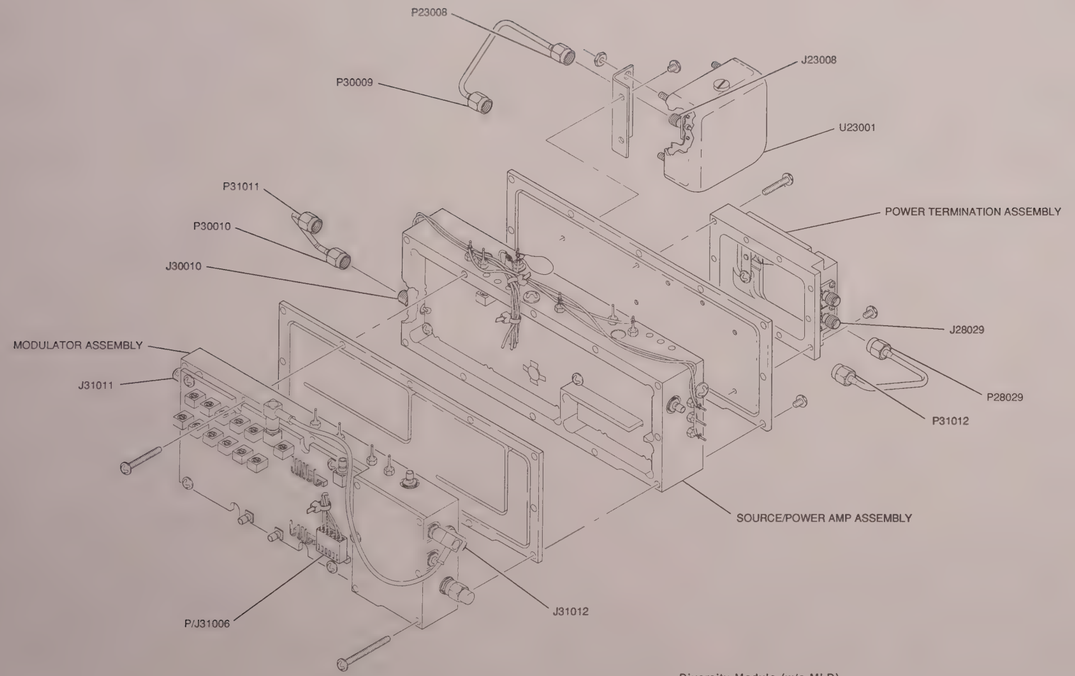
Motherboard PC Board Assembly
(7010-7130-100 B3)



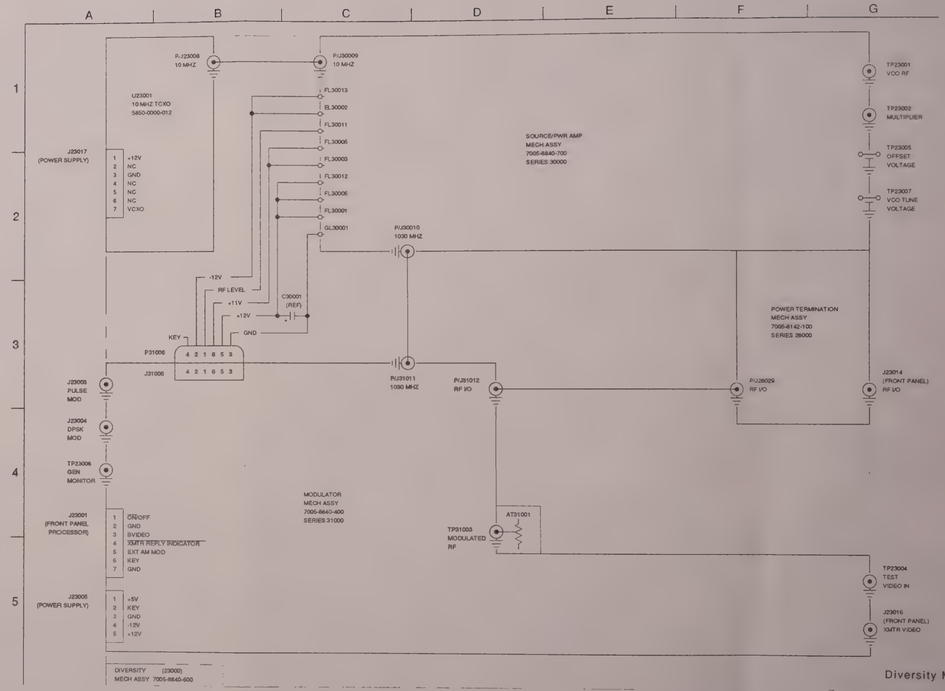
CAUTION

Motherboard PC Board Assembly
Figure 3-1

Motherboard PC Board Assembly Circuit Schematic

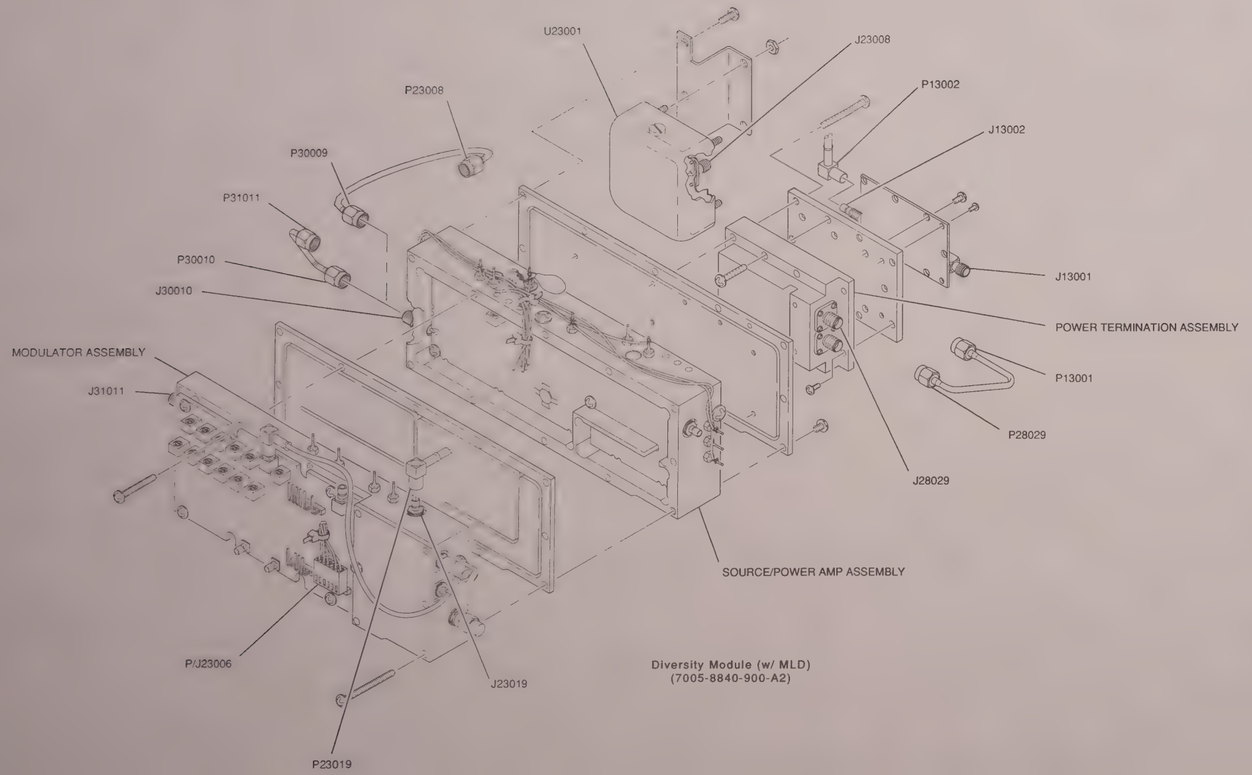



Diversity Module (w/o MLD)
(7005-8840-600-A4)

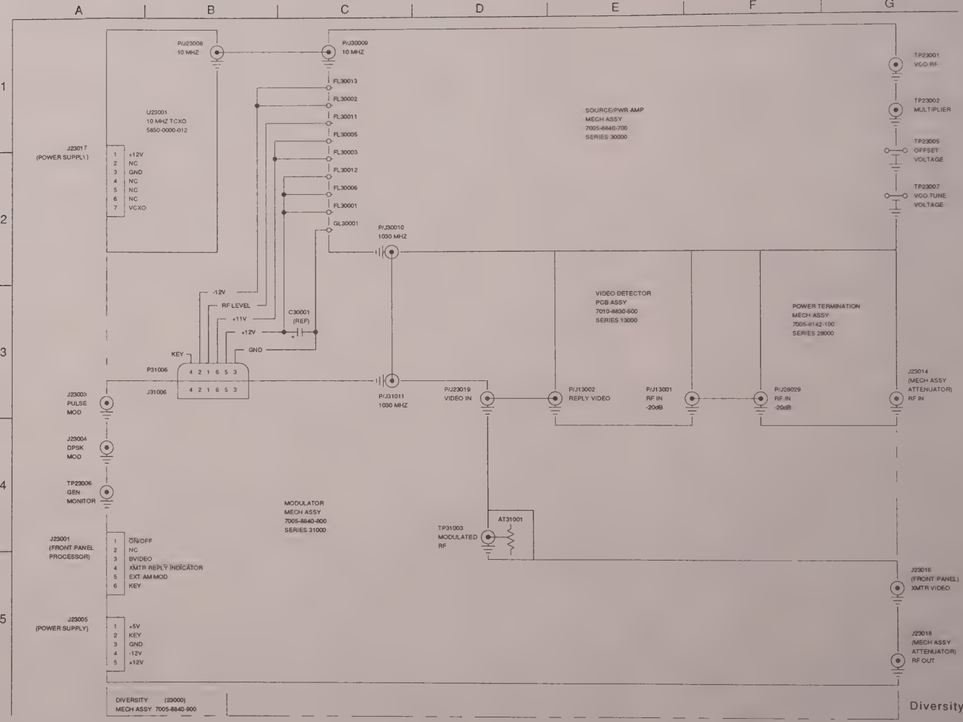



Diversity Module (w/o MLD) Interconnect Diagram
(0000-8840-600-A1)

Diversity Module (Sheet 1 of 9)
Figure 38

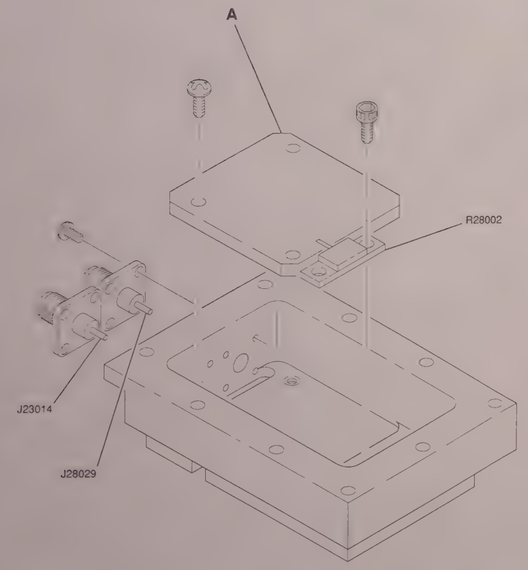



Diversity Module (w/ MLD)
(7005-8840-900-A2)

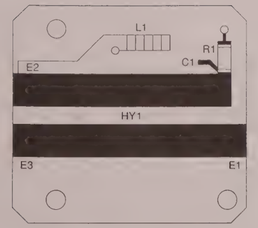



Diversity Module (Sheet 2 of 9)
Figure 38

Diversity Module (w/ MLD) Interconnect Diagram
(0000-8840-900-A1)

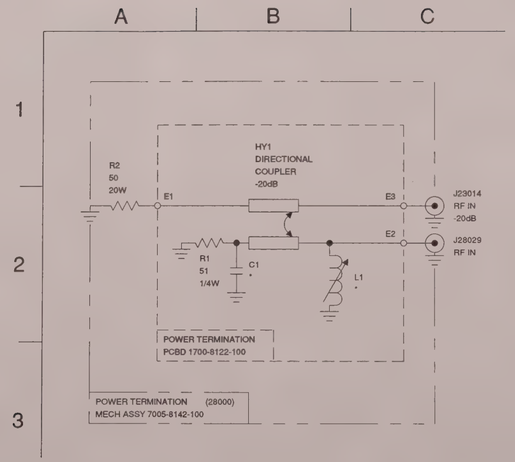



Power Termination Assembly
(7005-8142-100-B2)

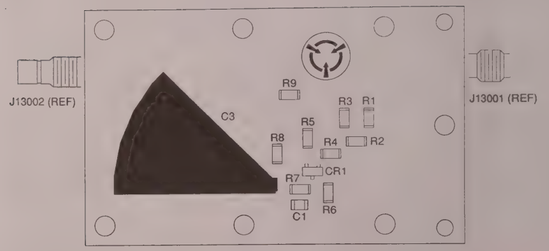



DETAIL **A**

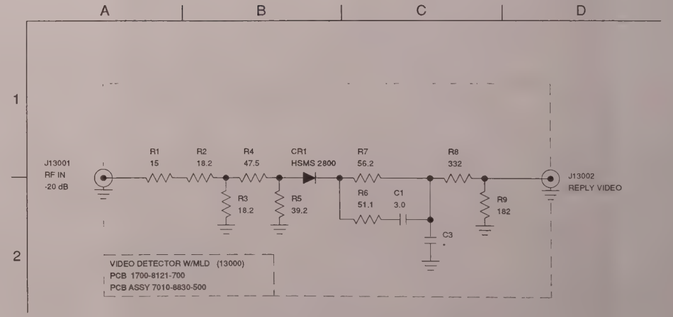
Power Termination PC Board



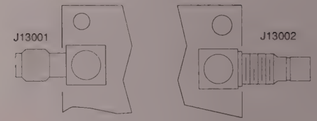

Power Termination Assembly Circuit Schematic
(0000-8142-100-B)




Video Detector Assembly
(7010-8830-500-C2)




Video Detector Assembly Circuit Schematic
(0000-8830-500-C)



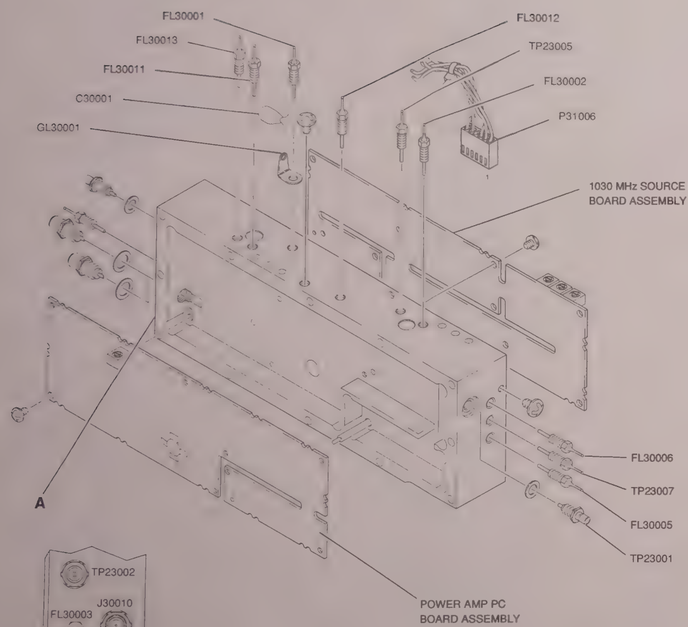

BOTTOM

**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A 7005-8142-100 28000 (e.g. R2 IS R28002).
   B 7010-8830-500 13000 (e.g. R1 IS R13001).
2. 7010-8830-500 ALL RESISTORS ARE 1/8W, 1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. 7010-8830-500 ALL CAPACITANCE IS EXPRESSED IN PICOFARADS.
5. 7010-8830-500 ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

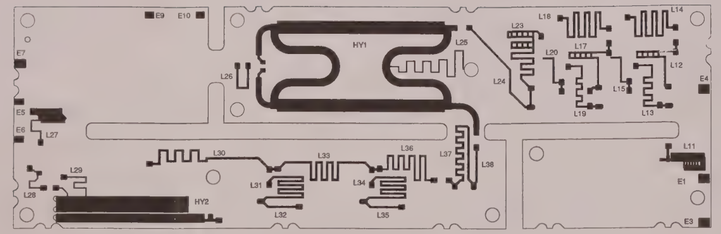
* - INDICATES TRANSMISSION LINES OF OTHER THAN 50 OHMS IMPEDANCE WHICH CONSTITUTE CIRCUIT ELEMENTS.

Diversity Module (Sheet 3 of 9)
Figure 38

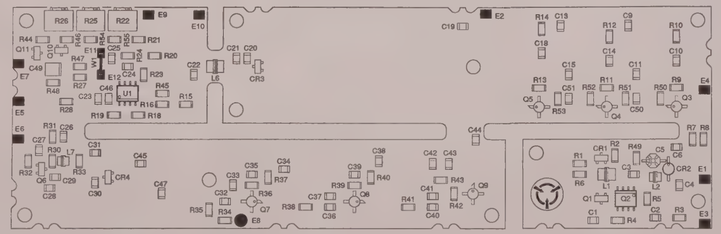


DETAIL **A**

Source/Pwr Amp Assembly
(7005-8840-700-E1)




TOP (PRINTED CIRCUITS)



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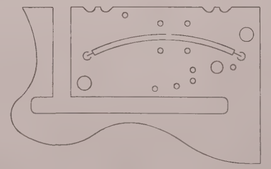
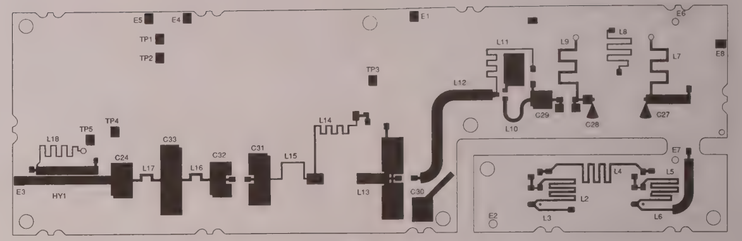
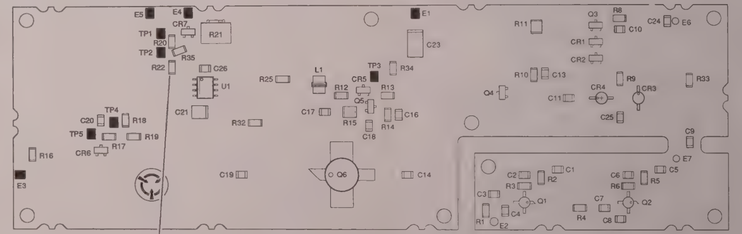


BOTTOM

1030 MHz Source PC Board Assembly
(7010-6830-400-E4)




TOP (PRINTED CIRCUITS)



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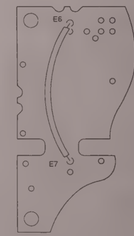
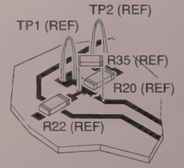


BOTTOM

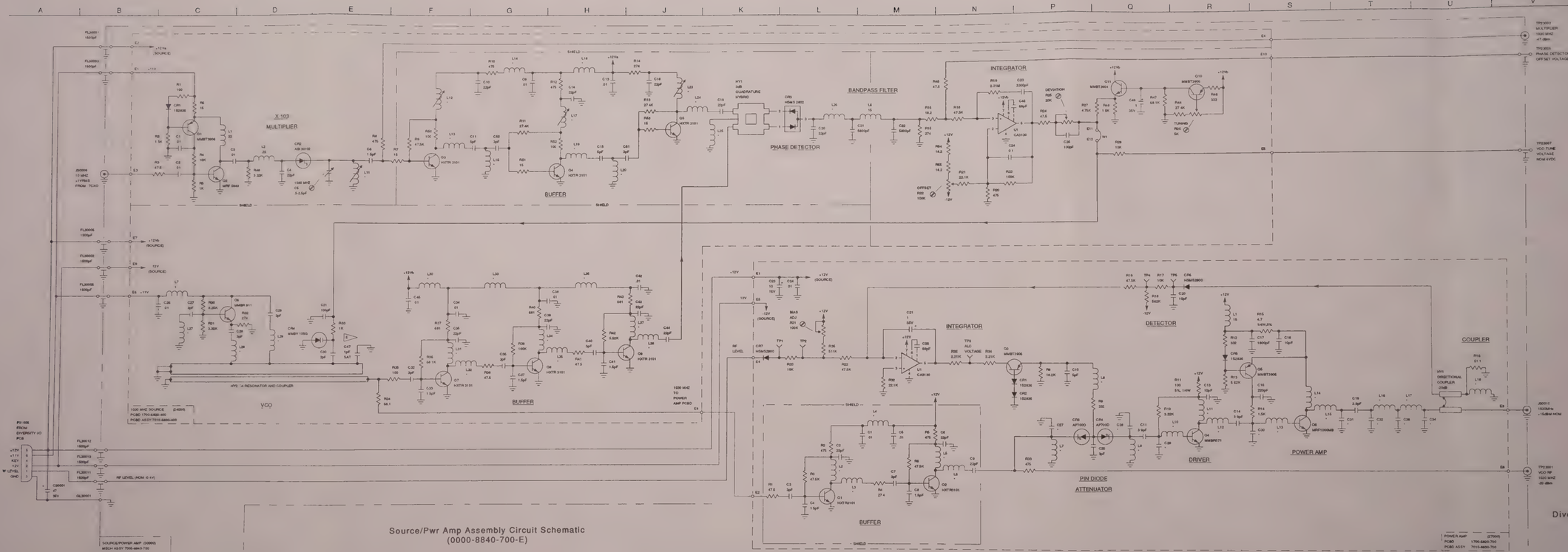
B




DETAIL **B**

Power Amp PC Board Assembly
(7010-8830-700-E1)

Diversity Module (Sheet 4 of 9)
Figure 38



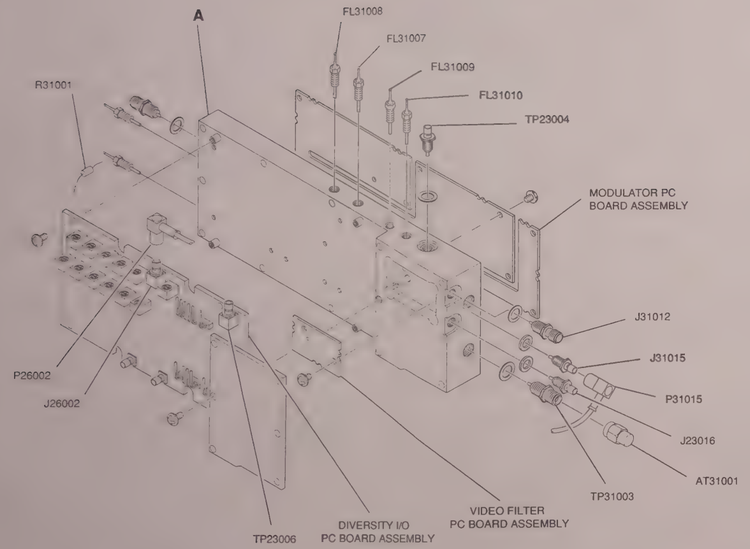

Source/Pwr Amp Assembly Circuit Schematic
(0000-8840-700-E)

**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)

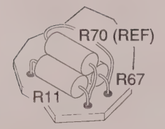
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   - A. 7005-8840-700 : 30000 (e.g. GL1 IS GL30001).
   - B. 7010-6830-400 : 24000 (e.g. C1 IS C24001).
   - C. 7010-8830-700 : 27000 (e.g. C1 IS C27001).
2. ALL RESISTORS ARE 1/8W, 1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. C24047 IS SELECT AT TEST. NORMAL VALUE IS 1.0pF, RANGE IS .4 TO 1.5pF.

Diversity Module (Sheet 5 of 9)
Figure 38

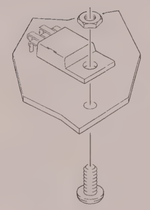



Modulator Assembly (w/o MLD)
(7005-8840-400-A)

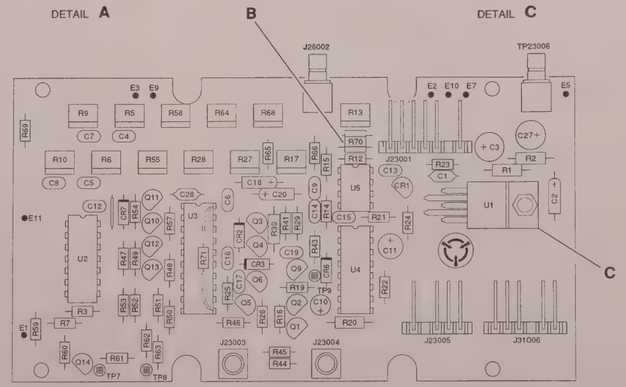
DETAIL A



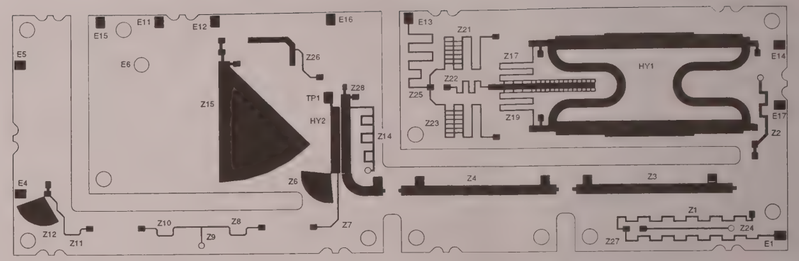

DETAIL B



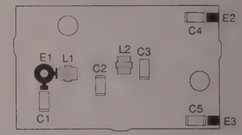
DETAIL C



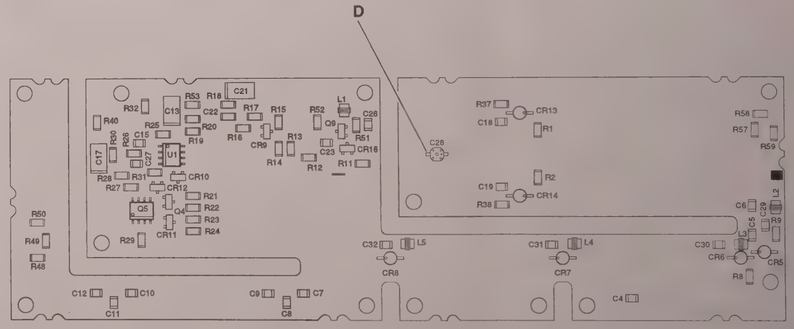

Diversity I/O PC Board Assembly
(7010-8830-300-A2)




TOP (PRINTED CIRCUITS)

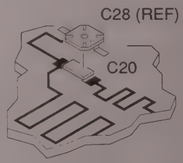



Video Filter PC Board Assembly
(7010-6830-900-D3)



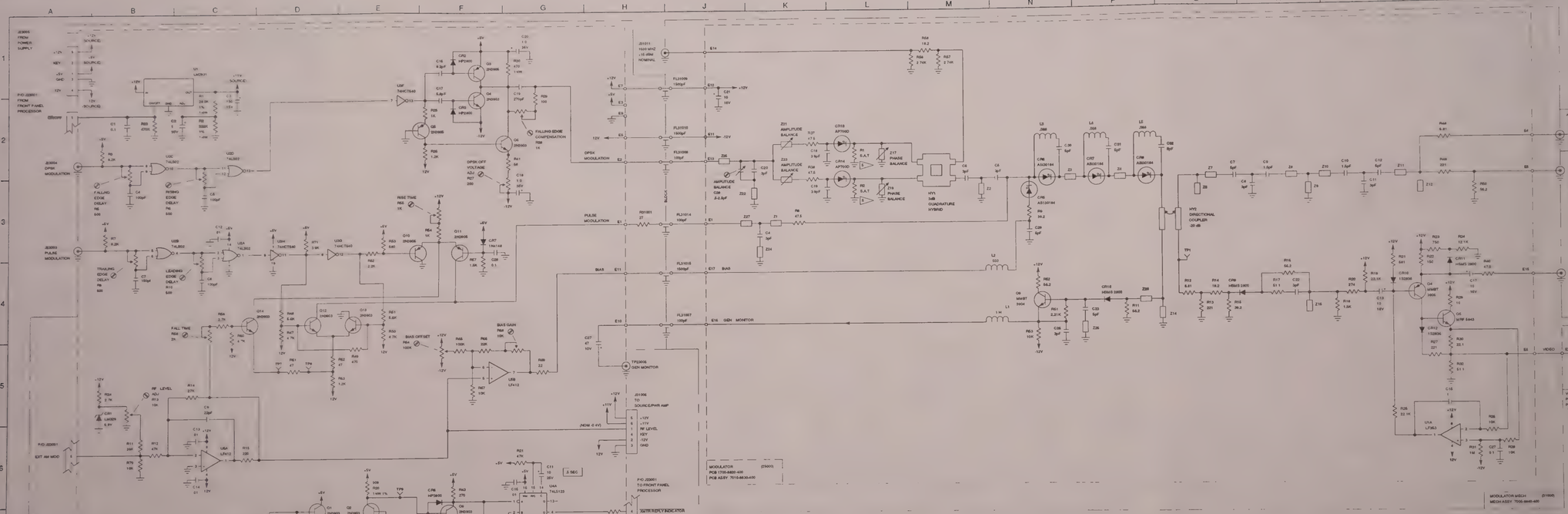

TOP

Modulator PC Board Assembly (w/o MLD)
(7010-8830-400-B1)



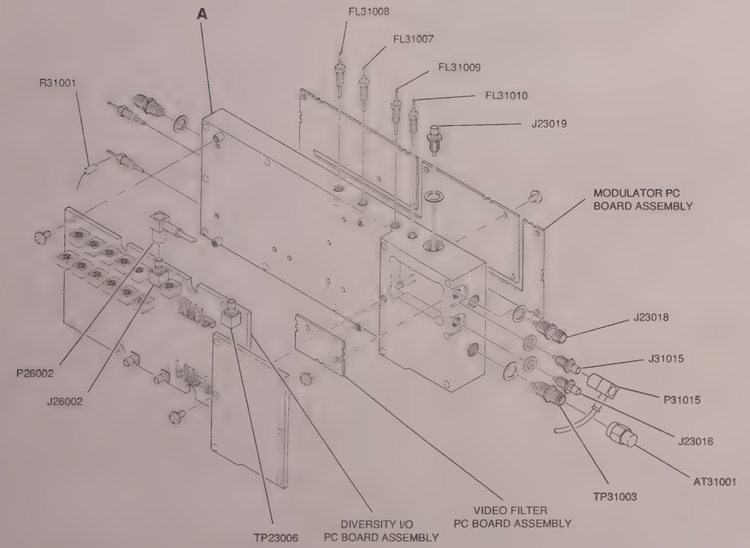

DETAIL D

Diversity Module (Sheet 6 of 9)
Figure 38


J3305 FROM POWER SUPPLY
P/O J23001 FROM FRONT PANEL PROCESSOR
J3304 DPSK MODULATION
J3303 PULSE MODULATION
J3302 EXT AM MOD
J3301 XMTR VIDEO
DIVERSITY I/O (D8000) PCB# 7700-8620-300 PCB ASSY 7010-8-630-300
PULSE MODULATION
DPSK MODULATION
BIAS
GDN MONITOR
FALLING EDGE COMPENSATION
DPSK OFF VOLTAGE ADJ
AMPLITUDE BALANCE
PHASE BALANCE
HYB1 3dB QUADRATURE HYBRID
HY2 DIRECTIONAL COUPLER -20 dB
TP1
TP3004 VIDEO INPUT
VIDEO FILTER (3800) PCB# 7700-8630-600 PCB ASSY 7010-8630-600
J3001 XMTR VIDEO TO FRONT PANEL 2V NOM. INTO 50
XMTR VIDEO A2
RF LEVEL ADJ
BIAS OFFSET
BIAS GAIN
BIAS ADJ
FALL TIME
TRAILING EDGE DELAY
LEADING EDGE DELAY
RISE TIME
XMTR REPLY INDICATOR
MODULE INSTALLED
S VIDEO
MODULATOR PCB 7700-8800-400 PCB ASSY 7010-8630-400
MODULATOR MECH (D1000) MECH ASSY 7006-8440-400
CAUTION:
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).
NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
A. 7005-8640-400 : 31000 (e.g. TP1 IS TP31001).
B. 7010-8830-900 : 29000 (e.g. C1 IS C29001).
C. 7010-8830-300 : 26000 (e.g. R1 IS R26001).
D. 7010-8830-400 : 25000 (e.g. R1 IS R25001).
2. 7010-8830-300 ALL RESISTORS ARE 1/8W, 5% TOLERANCE. 7010-8830-400 ALL RESISTORS ARE 1/8W, 1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5. R1 AND R2 ARE SELECT AT TEST. NORMAL VALUE IS 1kΩ. RANGE IS 1kΩ TO 10kΩ.

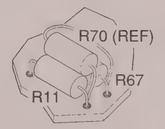
Modulator Assembly (w/o MLD) Circuit Schematic
(0000-8840-400-A2)

Diversity Module (Sheet 7 of 9)
Figure 38

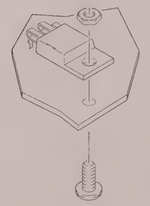



Modulator Assembly (w/ MLD)
(7005-8840-800-A1)

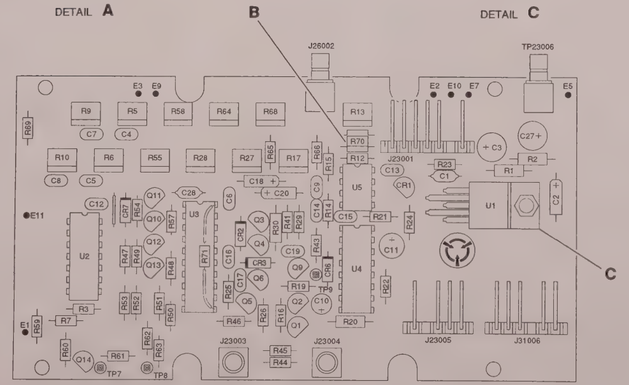
DETAIL A



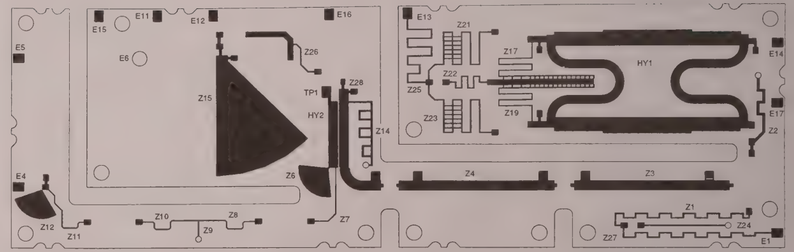

DETAIL B



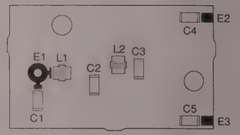
DETAIL C



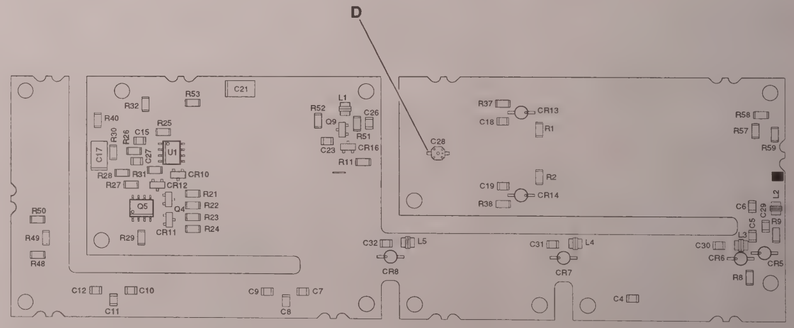

Diversity I/O PC Board Assembly
(7010-8830-300-A1)




TOP (PRINTED CIRCUITS)




Video Filter PC Board Assembly
(7010-6830-900-D3)

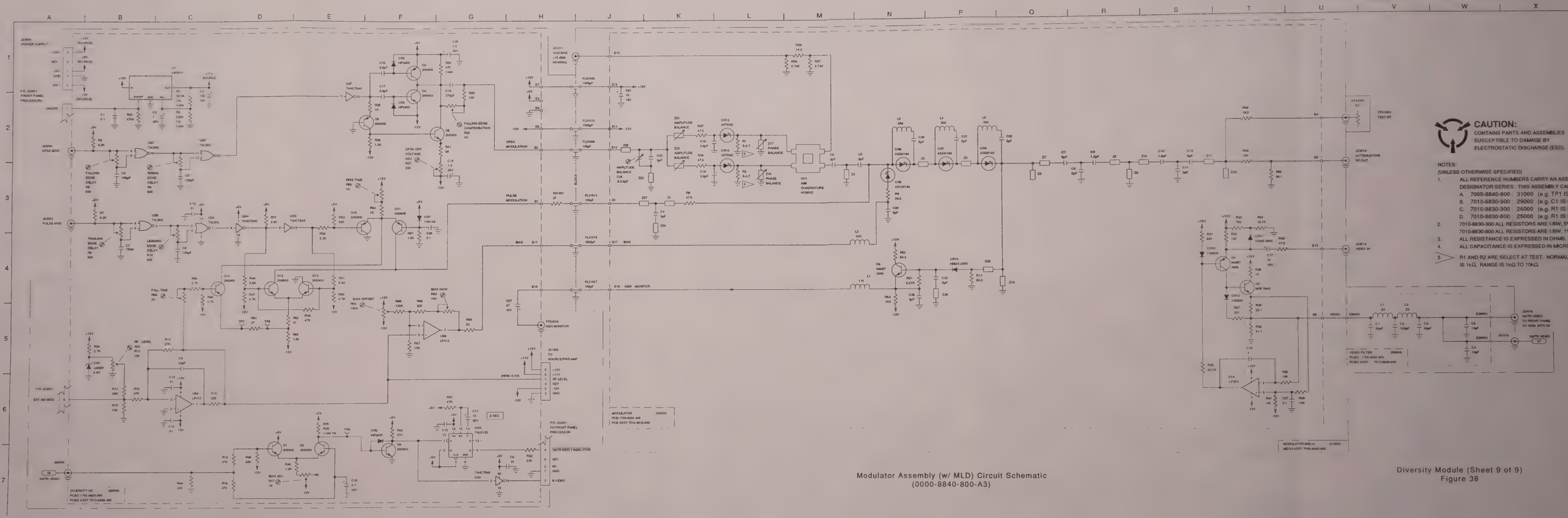



TOP

Modulator PC Board Assembly (w/ MLD)
(7010-8830-800-B1)

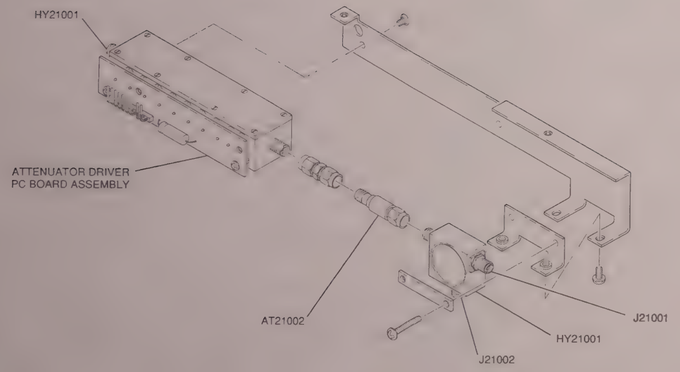
DETAIL D

Diversity Module (Sheet 8 of 9)
Figure 38

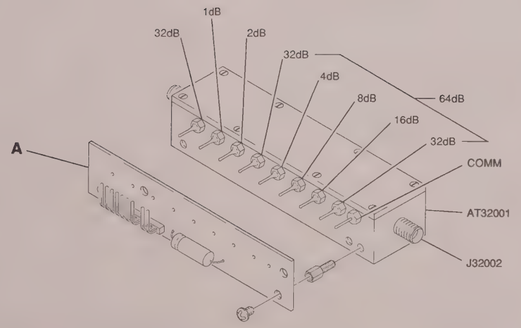

CAUTION:
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).
NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
A. 7005-8840-800 : 31000 (e.g. TP1 IS TP31001).
B. 7010-8830-900 : 29000 (e.g. C1 IS C29001).
C. 7010-8830-300 : 26000 (e.g. R1 IS R26001).
D. 7010-8830-800 : 25000 (e.g. R1 IS R25001).
2. 7010-8830-300 ALL RESISTORS ARE 1/8W, 5% TOLERANCE.
7010-8830-800 ALL RESISTORS ARE 1/8W, 1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.
5 R1 AND R2 ARE SELECT AT TEST. NORMAL VALUE IS 1kΩ. RANGE IS 1kΩ TO 10kΩ.
J33005 +POWER SUPPLY+
P-O J33001 FRONT PANEL PROCESSOR
J33004 DPSK MOD
J33003 PULSE MOD
P-O J33001 EXT AM MOD
J33002 XMTR VIDEO
DIVERSITY I/O PCB: 1700-4820-300 PCB ASSY: 7010-8430-300
J33001 TO FRONT PANEL PROCESSOR
J31001 1030 MHZ +15 dBM NOMINAL
J33006 TO SOURCE/PWR AMP
MODULATOR PCB 1700-4822-400 PCB ASSY 7010-8830-400
MODULATOR MECH MECH ASSY 7005-8840-800
J33014 ATTENUATOR RF OUT
J33019 VIDEO IN
J33016 XMTR VIDEO TO FRONT PANEL 2V PEAK INTO 93
XMTR VIDEO
VIDEO FILTER PCB: 1700-4820-900 PCB ASSY 7010-8430-900
DPSK MODULATION
PULSE MODULATION
BIAS
GEN MONITOR
BLOCK
VIDEO
RF LEVEL ADJ
FALL TIME
BIAS OFF/SET
BIAS GAIN
RISE TIME
FALLING EDGE COMPENSATION
DPSK OFF VOLTAGE ADJ
AMPLITUDE BALANCE
PHASE BALANCE
QUADRATURE HYBRID
3dB
FALLING EDGE DELAY
TRAILING EDGE DELAY
LEADING EDGE DELAY
RISING EDGE DELAY
BIAS ADJ
MTR REPLY INDICATOR
A SEC
TP3 1030 TEST PT
TP2006 GEN MONITOR

Modulator Assembly (w/ MLD) Circuit Schematic
(0000-8840-800-A3)

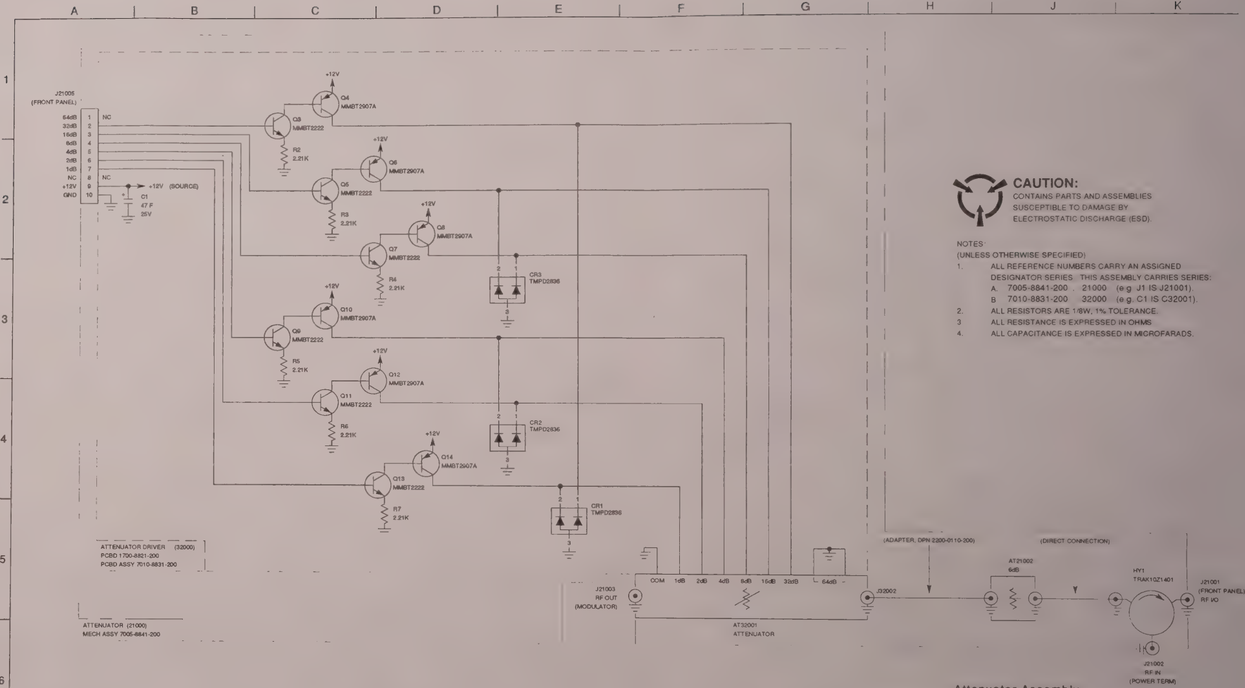
Diversity Module (Sheet 9 of 9)
Figure 38




Attenuator Assembly
(7005-8841-200-A1)




Attenuator Driver PC Board Assembly
(7010-8831-200-A)




**CAUTION:**
CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD).

NOTES:
(UNLESS OTHERWISE SPECIFIED)
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS ASSEMBLY CARRIES SERIES:
   A. 7005-8841-200 . . 21000 (e.g. J1 IS J21001).
   B. 7010-8831-200 . . 32000 (e.g. C1 IS C32001).
2. ALL RESISTORS ARE 1/8W, 1% TOLERANCE.
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

Attenuator Assembly Circuit Schematic
(0000-8841-200-A)

Attenuator Assembly
Figure 39

# SECTION 3 - DISASSEMBLY/REASSEMBLY

## 1. Disassembly

### A. General

Contains instructions necessary to remove and disassemble assemblies within the S-1403C.


| PROCEDURE | PAGE |
|---|---|
| Chassis Assembly | 5 |
| Power Supply Assembly | 5 |
| Line Supply PC Board Assembly | 9 |
| Processor and Pulse PC Board Assemblies | 10 |
| Front Panel Assembly | 11 |
| Diversity Module | 14 |
| Motherboard PC Board Assembly | 27 |
| Attenuator Assembly (w/ MLD) | 28 |


### B. Preliminary Considerations

(1) Tools Required

| TOOL | SIZE | DESCRIPTION |
|---|---|---|
| SCREWDRIVER | #1 #2 | PHILLIPS |
| SCREWDRIVER | #2 | SLOTTED |
| WRENCH | 1/4" 3/16" 7/16" 1/2" | SOCKET |
| WRENCH | 3/32" 0.05" | ALLEN |
| WRENCH | 1/4" 3/16" 5/16" | OPEN |
| SOLDERING IRON | N/A | PIN-TYPE |

Disassembly Tools
Table 1

(2) Disassembly Precautions

**CAUTION:** TAG EACH WIRE AND CABLE PRIOR TO REMOVAL.

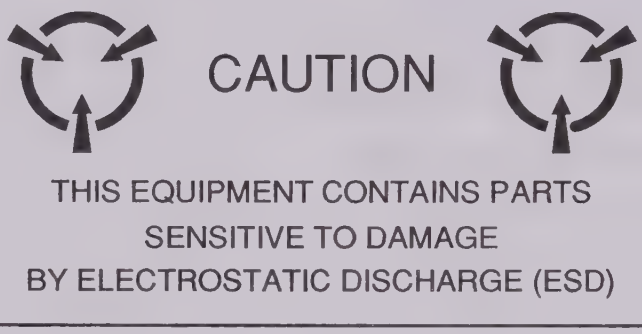
**CAUTION:** DO NOT BEND NOR TWIST SEMI-RIGID COAXIAL CABLES.

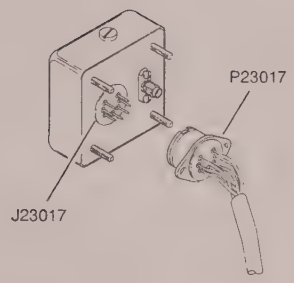
**CAUTION:** DO NOT PLACE UNDUE STRAIN ON ANY WIRE OR CABLE.

**CAUTION:** DO NOT DISCARD LOOSE ITEMS (NUTS, SCREWS, WASHERS, ETC.).

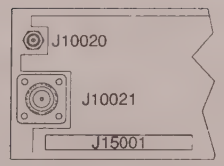
**CAUTION:** DO NOT EXPOSE COMPONENTS TO EXCESSIVE HEAT WHEN REMOVING SOLDER.

**CAUTION:** THE POWER SUPPLY ASSEMBLY, PROCESSOR PC BOARD ASSEMBLY, FRONT PANEL PROCESSOR PC BOARD ASSEMBLY, PULSE PC BOARD ASSEMBLY AND DIVERSITY MODULE CONTAIN PARTS SENSITIVE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD). ALL PERSONNEL PERFORMING DISASSEMBLY SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES.

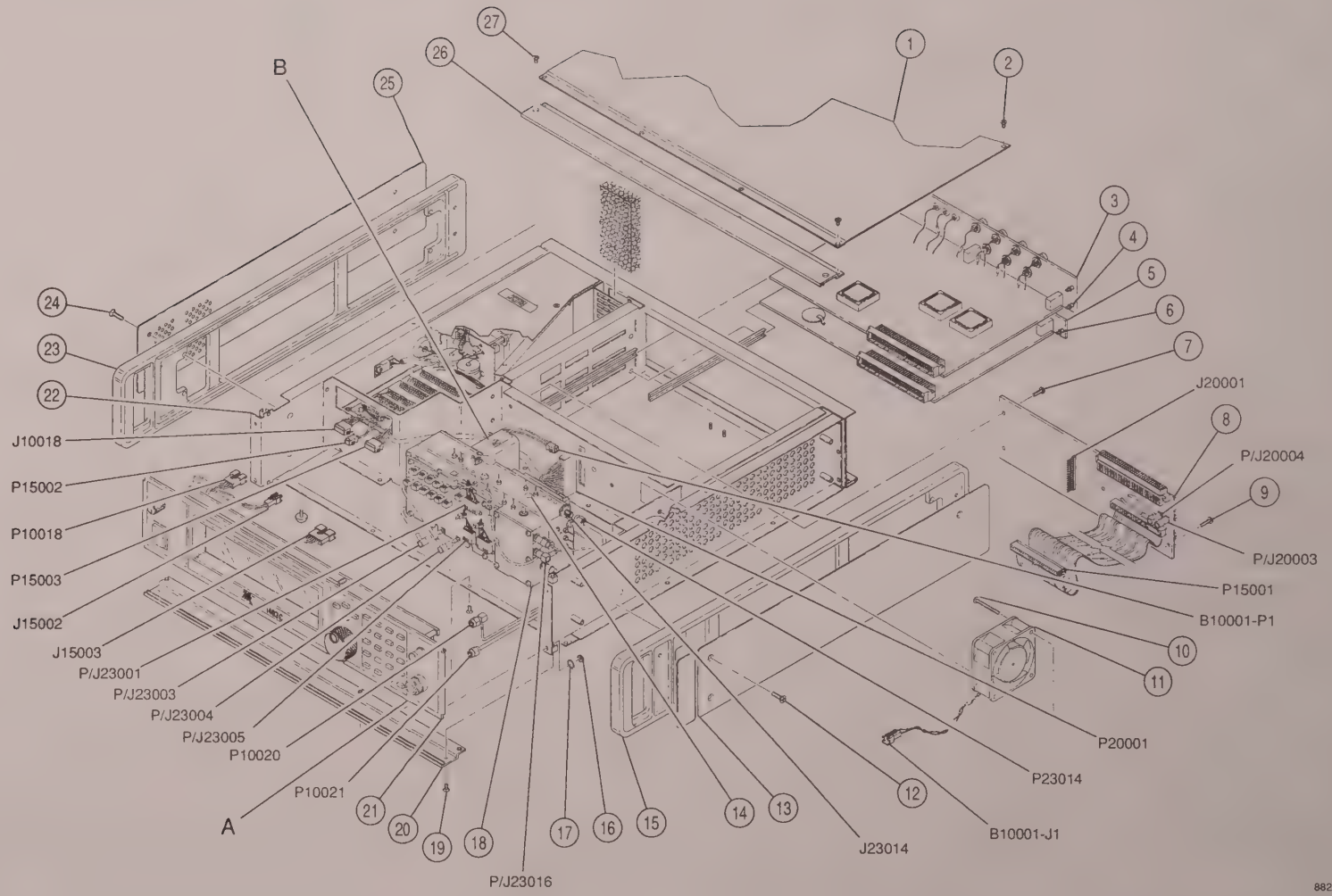




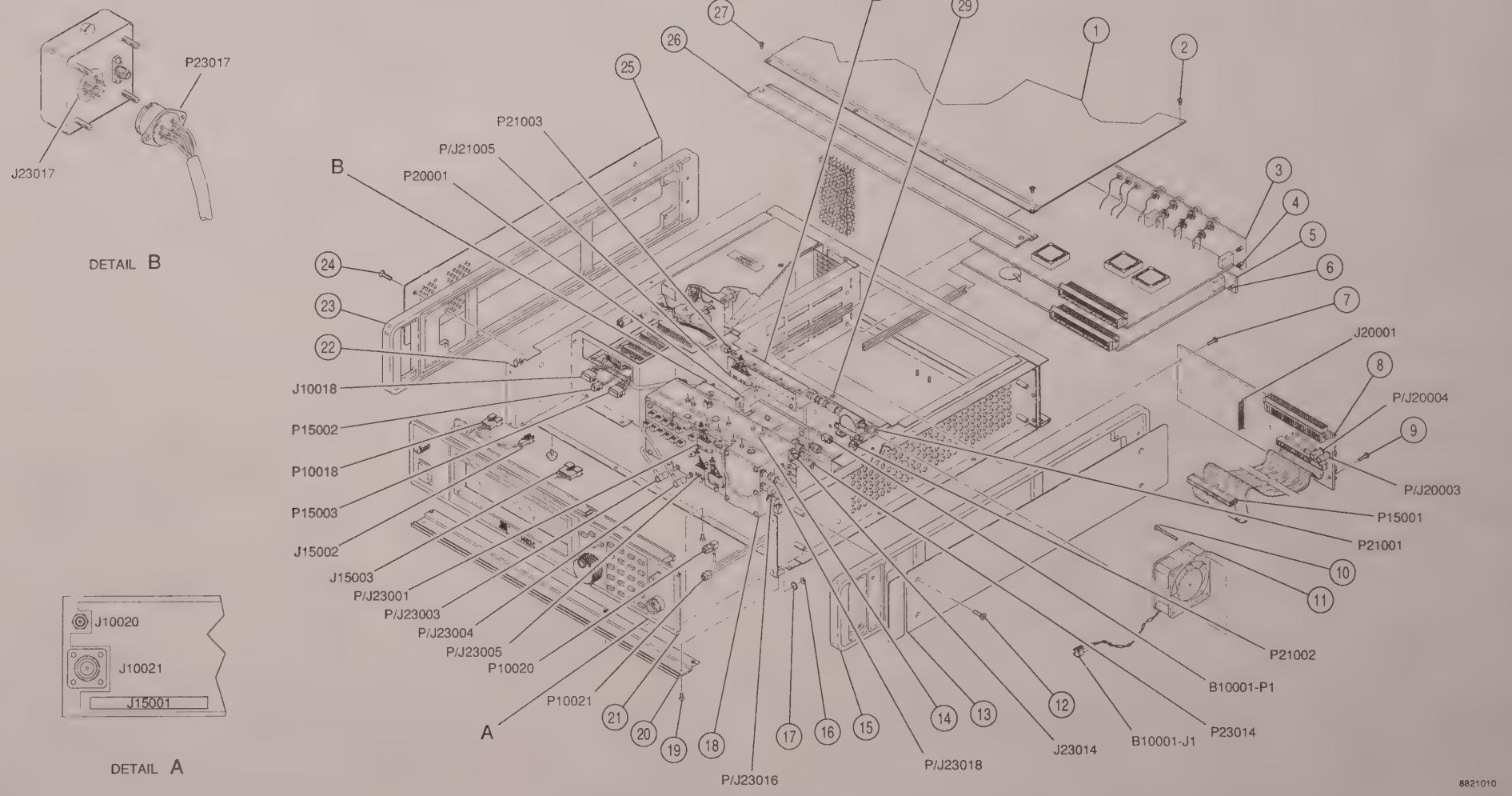

DETAIL B




DETAIL A




S-1403C Composite Disassembly (w/o MLD)
Figure 1




S-1403C Composite Disassembly (w/ MLD)
Figure 2

C. Disassembly Procedures

(1) Chassis Assembly

Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD).

| STEP | PROCEDURE |
|---|---|

1. Remove power from S-1403C.

**TOP COVER**

2. Remove two screws (2), one from middle of each side of top cover (1).
3. Remove two bracket screws (27).
4. Remove top cover (1) with top mounting bracket (26).

**SIDE RAILS**

5. Remove four screws (24) and left side rail (23) with cover (25).
6. Remove four screws (12) and right side rail (15) with cover (13).

**FAN**

7. Remove Diversity Module according to 2-3-1C(6).
8. Disconnect B10001-P1 (Power Supply Assembly) from B10001-J1 (Fan).
9. Remove four screws (10) and Fan (11).

(2) Power Supply Assembly

Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD), unless otherwise noted.

| STEP | PROCEDURE |
|---|---|

1. Remove top cover and left side rail according to 2-3-1C(1).
2. Disconnect cables as follows:
   - B10001-P1 (Power Supply Assembly) from B10001-J1 (Fan).
   - P23017 (Power Supply Assembly) from J23017 (Diversity Module).
   - P23005 (Power Supply Assembly) from J23005 (Diversity Module).
   - P15002 (Power Supply Assembly) from J15002 (Front Panel Assembly).
   - P15003 (Power Supply Assembly) from J15003 (Front Panel Assembly).
   - P20001 (Power Supply Assembly) from J20001 (Motherboard PC Board Assembly).

STEP PROCEDURE

**NOTE:** For Steps 3 through 5, refer to 2-3-1, Figure 3.

3. Remove two screws (4) and high voltage cover (3).

4. Disconnect P19001 (Power Supply Assembly) from J19001 (Line Supply PC Board Assembly).

5. Remove two screws (8) (middle of heat sink [7]) and lift Power Supply Assembly (5) from Chassis Assembly (6).

**POWER DISTRIBUTION PC BOARD ASSEMBLY**

**NOTE:** For Steps 6 through 17, refer to 2-3-1, Figure 4.

6. Remove six screws (14).

7. Remove screw (13), flat washer (12) and shoulder washer (11).

8. Cut plastic fasteners and place wires away from filter connections.

9. Remove solder from following filter connections on Power Distribution PC Board Assembly (10):

- FL18001 (E16007)
- FL18006 (E16003)
- FL18007 (E16006)
- FL18004 (E16002)
- FL18005 (E16005)
- FL18002 (E16001)
- FL18003 (E16004)

10. Remove Power Distribution PC Board Assembly (10).

**INVERTER SUPPLY PC BOARD ASSEMBLY**

11. Remove four screws (1) and Power Supply cover (2).

12. Remove four spacers (3).

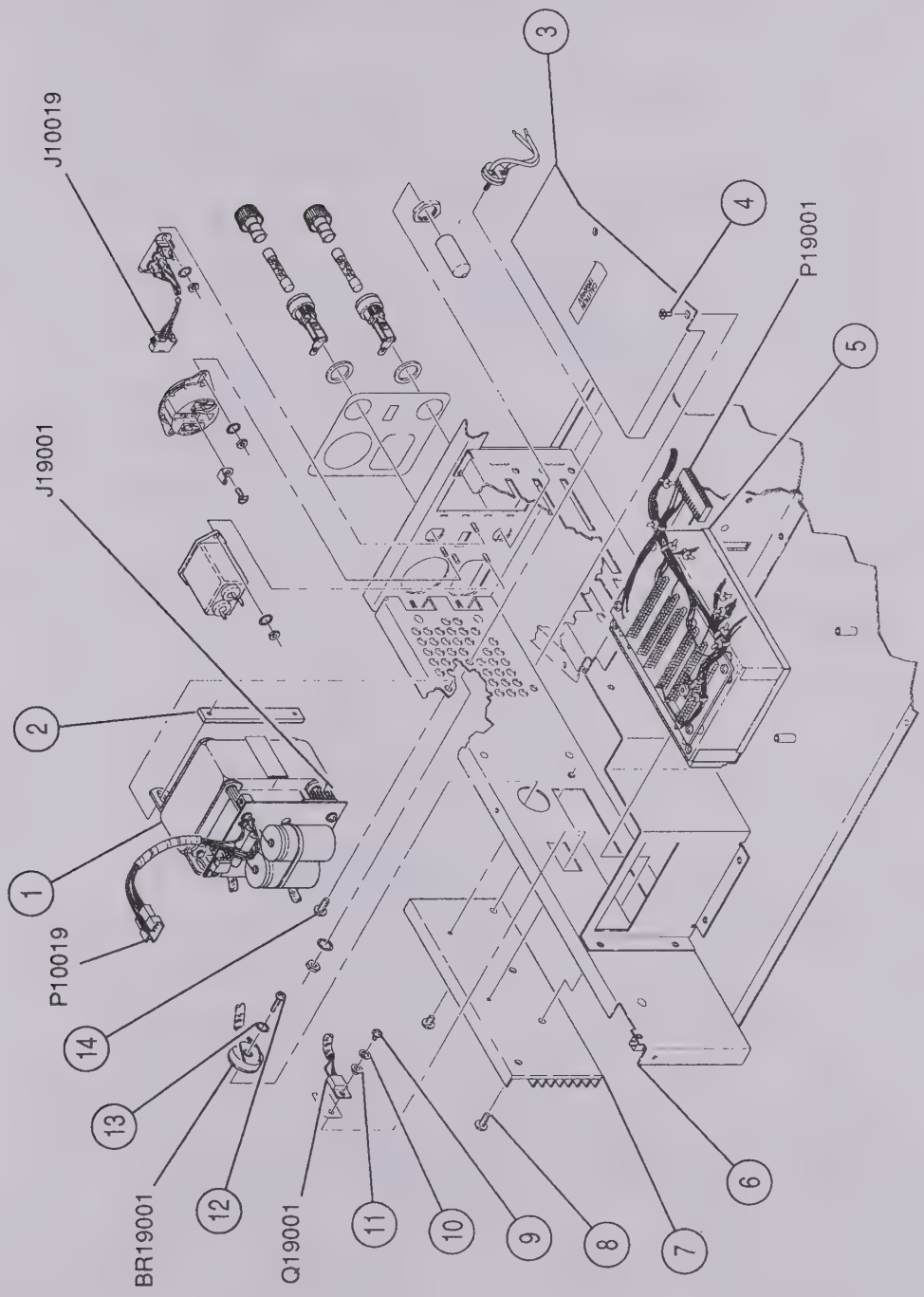
13. Remove four nuts (9), four split washers (8), four shoulder washers (6), four flat washers (5) and four screws (4).

**NOTE:** One screw faces the opposite direction.

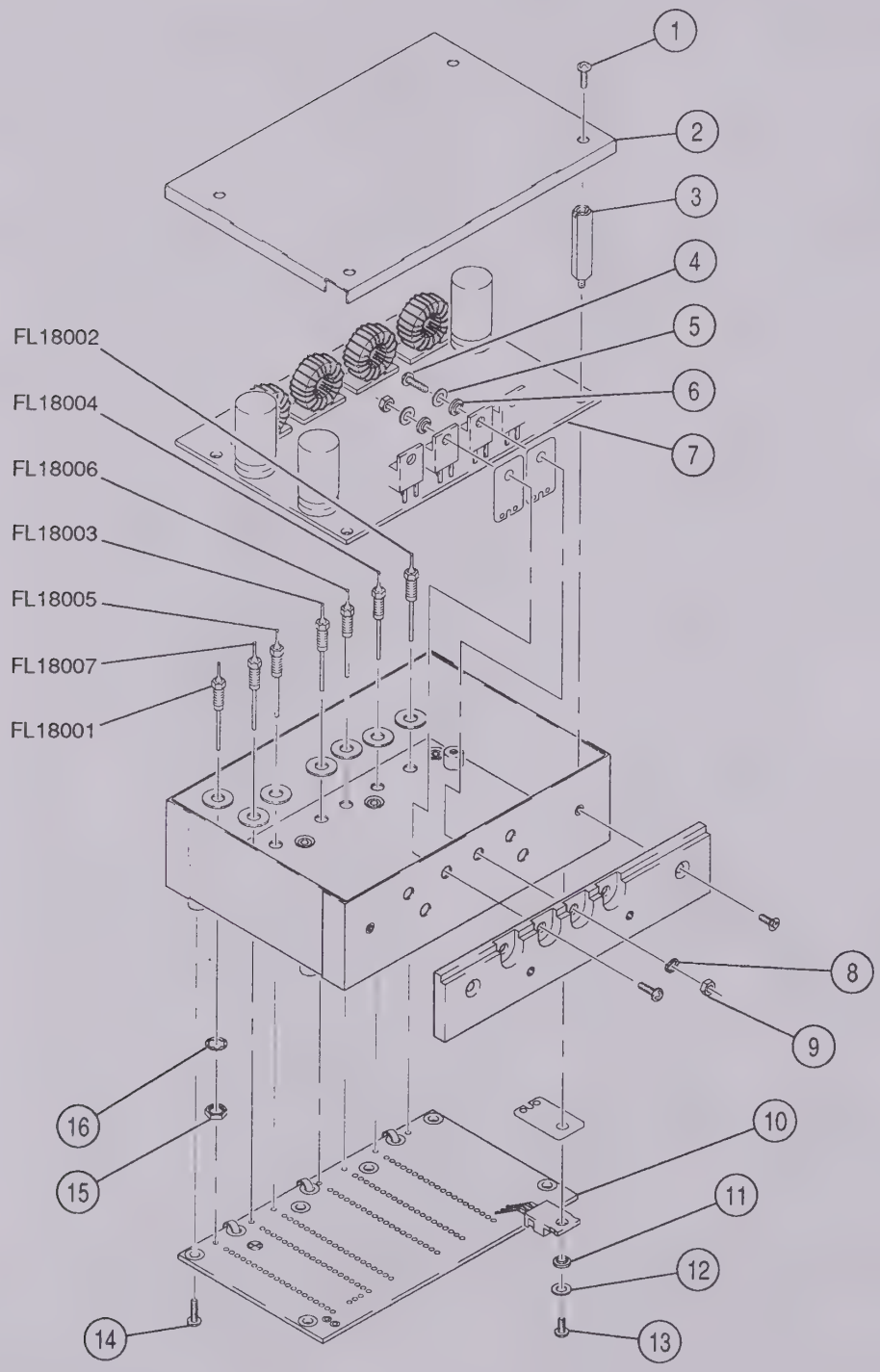
14. Remove solder from following filter connections on Inverter Supply PC Board Assembly (7):

- FL18001 (E17007)
- FL18006 (E17003)
- FL18007 (E17005)
- FL18004 (E17006)
- FL18005 (E17004)
- FL18002 (E17002)
- FL18003 (E17001)

8821008




Line Supply PC Board Assembly Disassembly
Figure 3




Power Supply Assembly Disassembly
Figure 4

| STEP | PROCEDURE |
|---|---|

15. Remove Inverter Supply PC Board Assembly (7).

**FILTERS**

16. Remove seven nuts (16) and seven washers (17).
17. Remove following filters:
    - FL18001
    - FL18006
    - FL18007
    - FL18004
    - FL18005
    - FL18002
    - FL18003

(3) Line Supply PC Board Assembly

Refer to 2-3-1, Figure 3.

| STEP | PROCEDURE |
|---|---|

1. Remove top cover and left side rail according to 2-3-1C(1).
2. Remove two screws (4) and high voltage cover (3).
3. Disconnect cables as follows:
    - P19001 (Power Supply Assembly) from J19001 (Line Supply PC Board Assembly).
    - P10019 (Line Supply PC Board Assembly) from J10019 (LINE SELECT Switch).
4. Remove screw (9), flat washer (10), shoulder washer (11) and Q19001 from Chassis Assembly (6).
5. Remove screw (12), lock washer (13) and BR19001 from Chassis Assembly (6).
6. Remove four screws (14) and two transformer brackets (2).
7. Remove Line Supply PC Board Assembly (1) from Chassis Assembly (6).

(4) Processor and Pulse PC Board Assemblies

Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD).

| STEP | PROCEDURE |
|---|---|

**PROCESSOR PC BOARD ASSEMBLY**

1. Release two DZUS fasteners (6).
2. Remove Processor PC Board Assembly (5) from Chassis Assembly (22).

**PULSE PC BOARD ASSEMBLY**

3. Release four DZUS fasteners (4).
4. Remove Pulse PC Board Assembly (3) from Chassis Assembly (22).

(5) Front Panel Assembly

Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD), unless otherwise noted.

| STEP | PROCEDURE |
|---|---|

1. Remove top cover and side rails according to 2-3-1C(1).
2. Remove four nuts (16) and four lock washers (17).
3. Loosen two screws (19) securing bottom mounting bracket (20).
4. Disconnect P10021 (Diversity Module or Attenuator Assembly [w/ MLD]) from J10021(to ANT B Connector).
5. Lower bottom mounting bracket (20) and remove Front Panel Assembly (21) from Chassis Assembly (22).
6. Disconnect cables as follows:
   - P10020 (Diversity Module) from J10020 (to UUT XMTR Connector).
   - P23001 (Front Panel Assembly) from J23001 (Diversity Module).
   - P15002 (Power Supply Assembly) from J15002 (Front Panel Assembly).
   - P15003 (Power Supply Assembly) from J15003 (Front Panel Assembly).
   - P10018 (Front Panel Assembly) from J10018 (AC IN Connector).
   - If MLD is installed, P15006 (Attenuator Assembly) from J15006 (Front Panel Assembly).
   - P15001 (Motherboard PC Board Assembly) from J15001 (Front Panel Assembly). Push tabs out to disconnect.

STEP PROCEDURE

**FRONT PANEL PROCESSOR PC BOARD ASSEMBLY**

**NOTE:** For Steps 7 through 14, refer to 2-3-1, Figure 5.

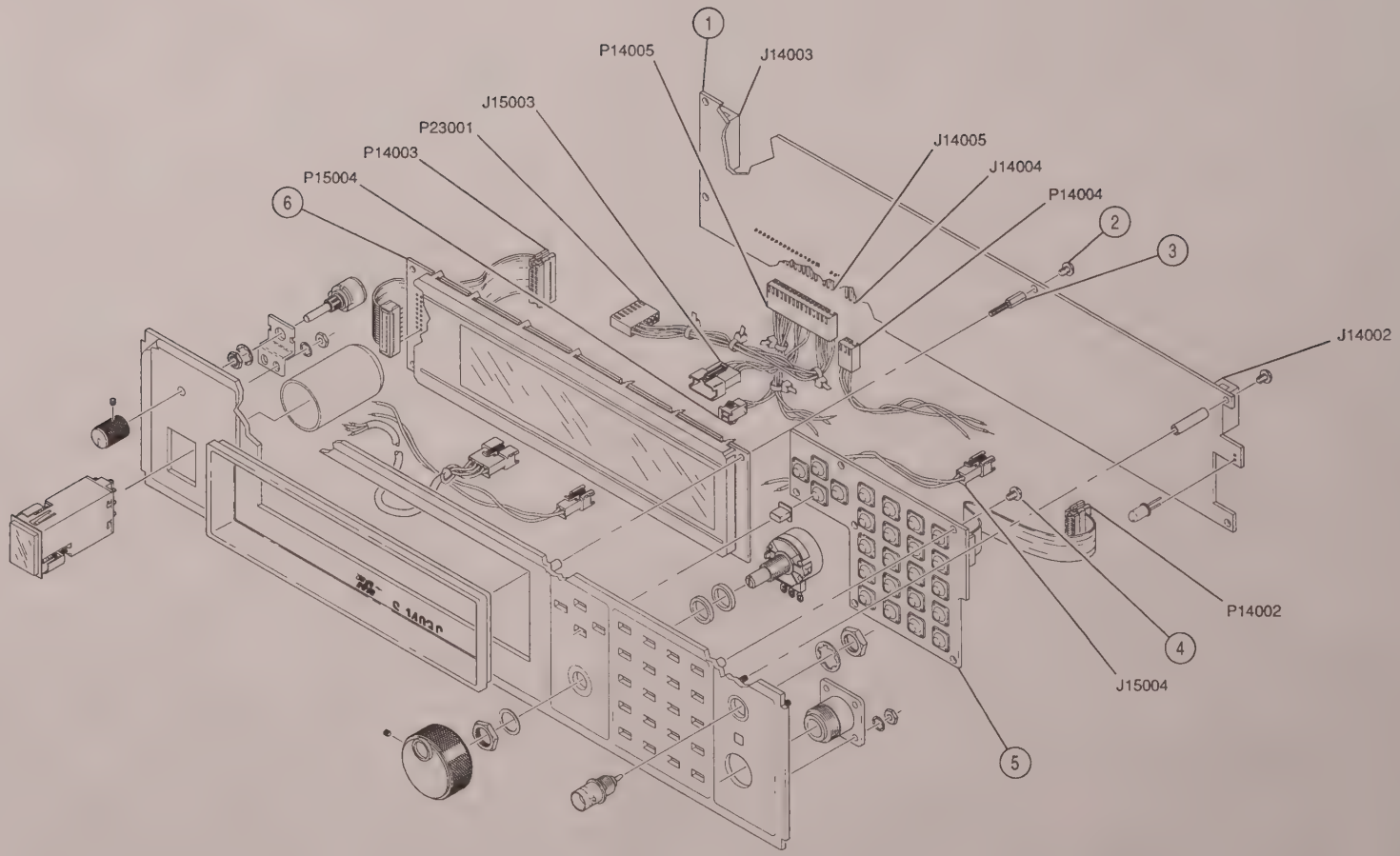
7. Disconnect cables as follows:
   - P14005 (P23001, J15003, BRIGHTNESS Control and P15004) from J14005 (Front Panel Processor PC Board Assembly).
   - P14004 (SLEW Control) from J14004 (Front Panel Processor PC Board Assembly).
   - P14003 (MENU Display) from J14003 (Front Panel Processor PC Board Assembly).
   - P14002 (Keyboard PC Board Assembly) from J14002 (Front Panel Processor PC Board Assembly).
8. Remove six screws (2).
9. Remove Front Panel Processor PC Board Assembly (1).

**KEYBOARD PC BOARD ASSEMBLY**

10. Remove six screws (4).
11. Remove Front Panel Processor PC Board Assembly (5).

**MENU DISPLAY**

12. Disconnect P15004 (Front Panel PC Board Assembly via P14005) from J15004 (MENU Display).
13. Remove four standoffs (3).
14. Remove MENU Display (6).




8821001

Front Panel Assembly Disassembly
Figure 5

(6) Diversity Module

Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD).

| STEP | PROCEDURE |
|---|---|

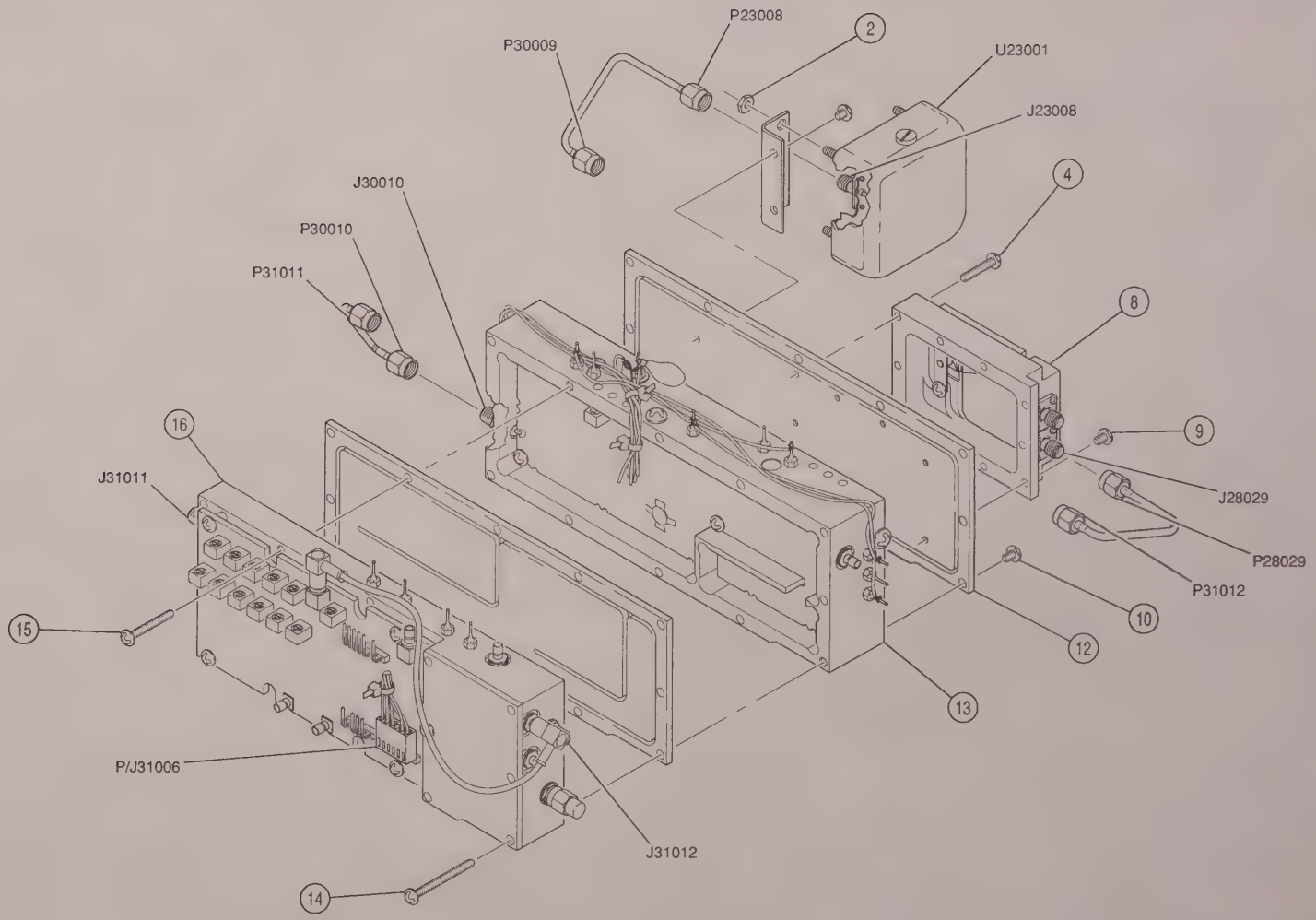
1. Remove top cover according to 2-3-1C(1).
2. Disconnect cables as follows:
   - P23001 (Front Panel Assembly) from J23001 (Diversity Module).
   - P23016 (Front Panel Assembly) from J23016 (Diversity Module).
   - P23005 (Power Supply Assembly) from J23005 (Diversity Module).
   - P23017 (Power Supply Assembly) from J23017 (Diversity Module).
   - P23003 (Motherboard PC Board Assembly) from J23003 (Diversity Module).
   - P23004 (Motherboard PC Board Assembly) from J23004 (Diversity Module).
   - P23014 (Front Panel Assembly or Attenuator Assembly [w/ MLD]) from J23014 (Diversity Module).
   - If MLD is installed, P23018 (Attenuator Assembly) from J23018 (Diversity Module).
3. Remove two screws (14).
4. Remove Diversity Module (18) from Chassis Assembly (22).

(a) Modulator Assembly

Refer to 2-3-1, Figure 6 (w/o MLD) or Figure 7 (w/ MLD), unless otherwise noted.

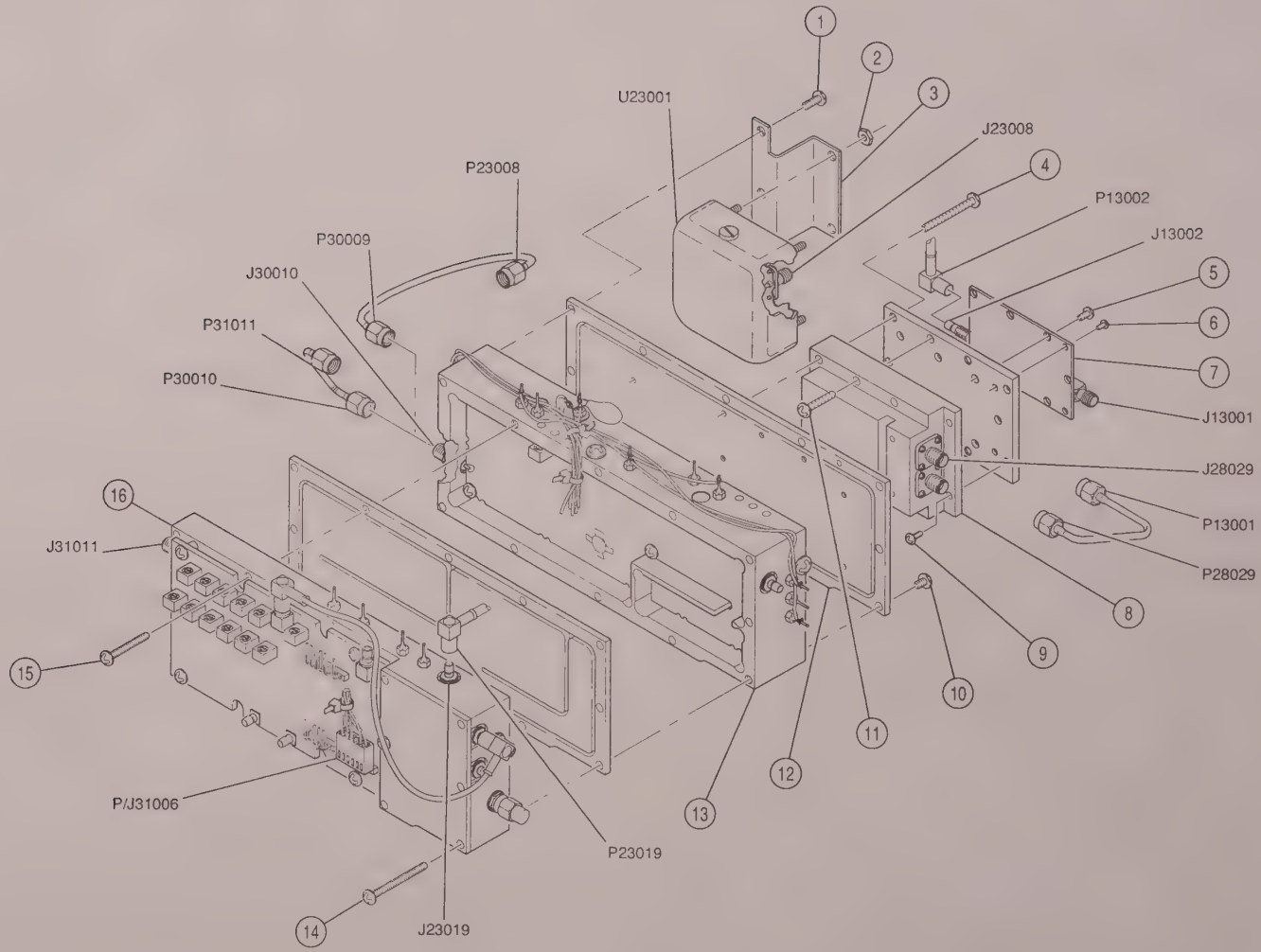
| STEP | PROCEDURE |
|---|---|

1. Remove Diversity Module according to 2-3-1C(6), Steps 1 through 4.
2. Disconnect cables as follows:
   - P31011 (Source Pwr Amp Assembly) from J31011 (Modulator Assembly).
   - P31006 (Source Pwr Amp Assembly) from J31006 (Diversity I/O PC Board Assembly).
   - If MLD is not installed, P31012 (Power Termination Assembly) from J31012 (Modulator Assembly).
   - If MLD is installed, P23019 (Video Detector PC Board Assembly) from J23019 (Modulator Assembly).




8821005

Diversity Module (w/o MLD)
Figure 6




8821006

Diversity Module (w/ MLD)
Figure 7

STEP PROCEDURE

3. Remove five long screws (14) (all located on outside perimeter) and seven medium length screws (15).

4. Remove Modulator Assembly (16).

**DIVERSITY I/O PC BOARD ASSEMBLY**

**NOTE:** For Steps 5 through 18, refer to 2-3-1, Figure 8.

5. Disconnect P26002 (Modulator Assembly) from J26002 (Diversity I/O PC Board Assembly).

6. Remove solder and disconnect as follows:

   - R31001 from FL31014.
   - Wire (E26011) from FL31015.
   - Wire (E26002) from FL31008.
   - Wire (E26010) from FL31007.
   - Wire (E26007) from FL31009.
   - Wire (E26005) from FL31010.

7. Remove four screws (8).

8. Remove Diversity I/O PC Board Assembly (7).

**VIDEO FILTER PC BOARD ASSEMBLY**

9. Disconnect P31015 (Diversity I/O PC Board Assembly) from J31015 (Modulator Assembly).

10. Remove one screw (6) and Video Filter cover (5).

11. Remove solder from following connections on Video Filter PC Board Assembly (3):

    - E29001
    - J31015 (E29002)
    - J23016 (E29003)

12. Remove J23016 and J31015 from Modulator Assembly.

13. Remove two screws (4).

14. Remove Video Filter PC Board Assembly (3).

STEP PROCEDURE

**MODULATOR PC BOARD ASSEMBLY**

15. Remove solder from following connections on Modulator PC Board Assembly (2):

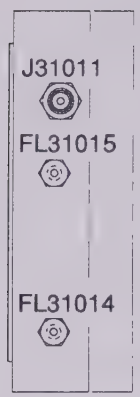
- FL31014 (E25001)
- J31012 (E25005)
- J31015 (E25006)
- TP23004 (E25015)
- FL31010 (E25011)
- AT31001/TP31003 (E25004)
- FL31009 (E25012)
- FL31007 (E25016)
- FL31008 (E25013)
- J31011 (E25014)
- FL31015 (E25017)

16. Remove following items from Modulator Assembly:

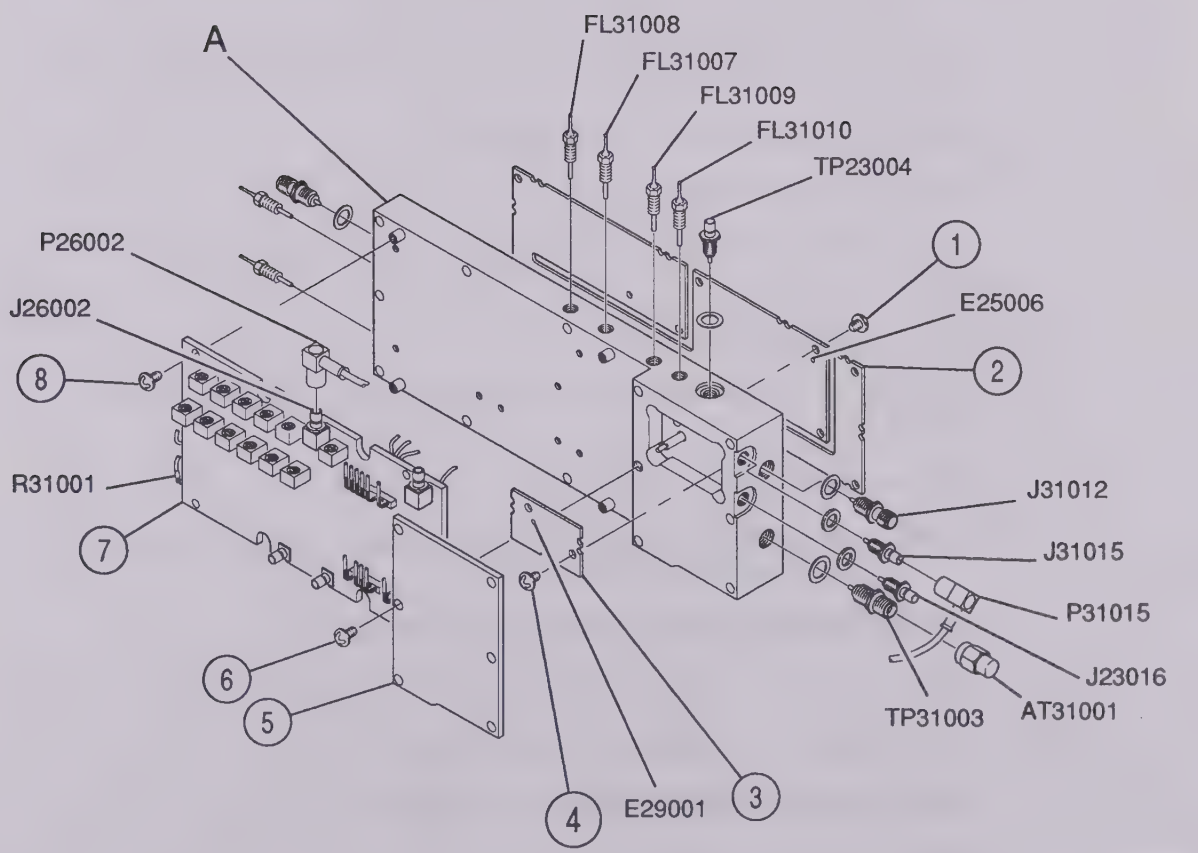
- FL31014
- J31015
- FL31010
- FL31009
- AT31001/TP31003
- J31012 (w/o MLD)/J23018 (w/ MLD)
- TP23004 (w/o MLD)/J23019 (w/ MLD)
- FL31007
- FL31008
- J31011
- FL31015

17. Remove 12 screws (1).

18. Remove Modulator PC Board Assembly (2).




DETAIL A




Modulator Assembly Disassembly
Figure 8

(b) Source/Pwr Amp Assembly

Refer to 2-3-1, Figure 6 (w/o MLD) or Figure 7 (w/ MLD), unless otherwise noted.

| STEP | PROCEDURE |
|---|---|

1. Remove Diversity Module according to 2-3-1C(6), Steps 1 through 4.
2. Disconnect cables as follows:
   - P30010 (Modulator Assembly) from J30010 (Source Pwr Amp Assembly).
   - P31006 (Source Pwr Amp Assembly) from J31006 (Diversity I/O PC Board Assembly).
   - If MLD is not installed, P28029 (Modulator Assembly) from J28029 (Power Termination Assembly).
   - If MLD is installed, P13002 (Modulator Assembly) from J13002 (Video Detector PC Board Assembly).
3. Remove five long screws (15) (all located on outside perimeter) and seven medium length screws (14).
4. Remove Source/Pwr Amp Assembly (13).

**10 MHz TCXO (U23001)**

5. Disconnect P23008 (Source/Pwr Amp Assembly) from J23008 (U23001).
6. Remove two nuts (2).
7. If MLD is installed, remove three screws (1) and TCXO mounting bracket (3).
8. Remove U23001 (10 MHz TCXO).

**NOTE:** Proceed with Steps 9, 10 and 18; if MLD is not installed. If MLD is installed, go to Step 11.

**POWER TERMINATION ASSEMBLY (w/o MLD)**

9. Remove five long screws (4) and two short screws (9).
10. Remove Power Termination Assembly (8).

**POWER TERMINATION ASSEMBLY (w/ MLD)**

11. Remove four screws (4).
12. Remove Power Termination Assembly (8) with Video Detector PC Board Assembly (5).

STEP PROCEDURE

13. Disconnect cable as follows:

    - P13001 (Power Termination Assembly) from J13001 (Video Detector PC Board Assembly).
    - P28029 (Video Detector PC Board Assembly) from J28029 (Power Termination Assembly).

14. Remove three medium length screws (11) and two short screws (9).

15. Remove Power Termination Assembly (8).

**VIDEO DETECTOR PC BOARD ASSEMBLY (w/ MLD)**

16. Remove seven short screws (5) and two small screws (6).

17. Remove Video Detector PC Board Assembly (7).

STEP PROCEDURE

**RESISTOR R28002**

**NOTE:** For Steps 18 through 25, refer to 2-3-1, Figure 9.

18. Remove two socket head screws (1).

19. Remove solder from connection between R28002 (3) and Power Termination PC Board (2).

20. Remove R28002 (3) from Power Termination Assembly (4).

**CONNECTORS J28029 AND J23014**

21. Remove four screws (5).

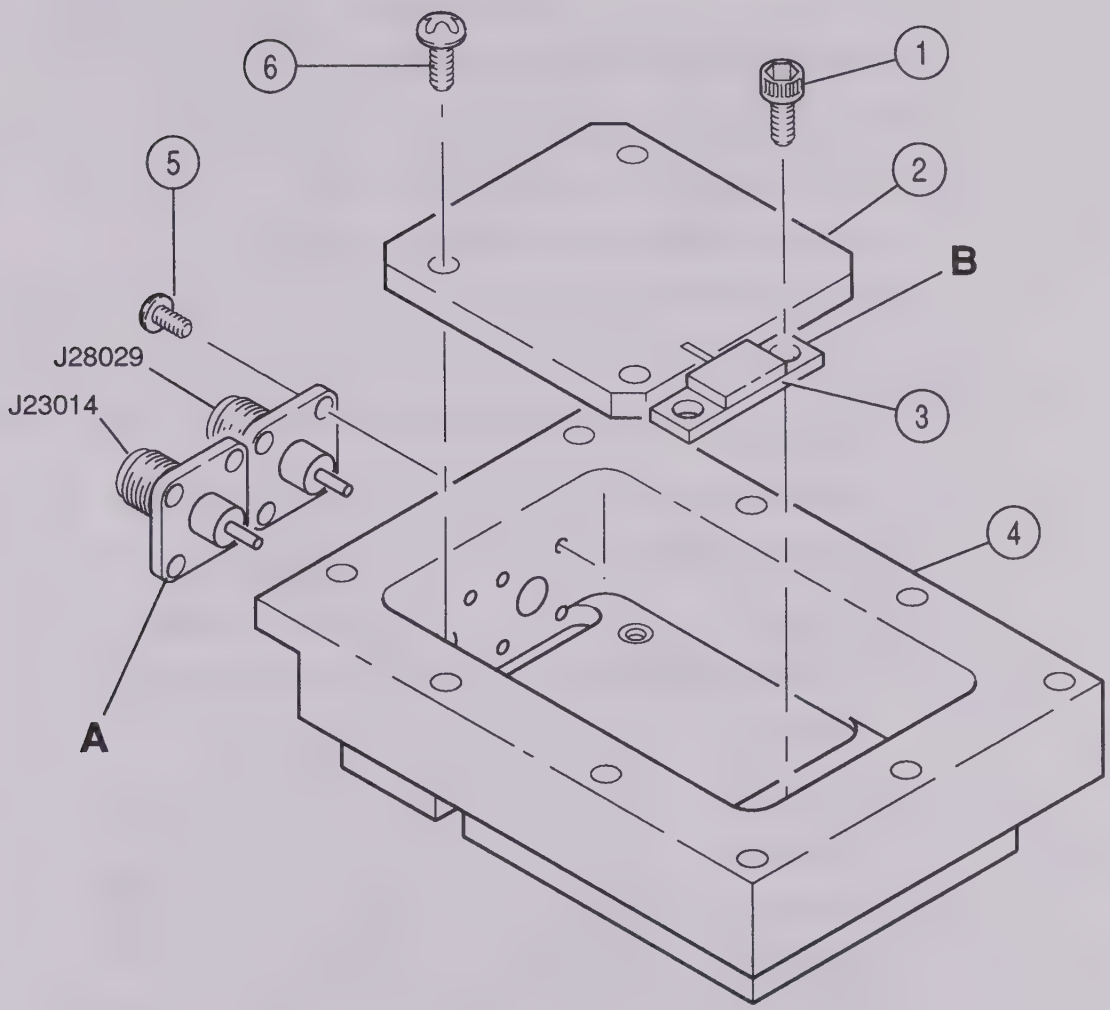
22. Remove solder from connection between connector and Power Termination PC Board (2).

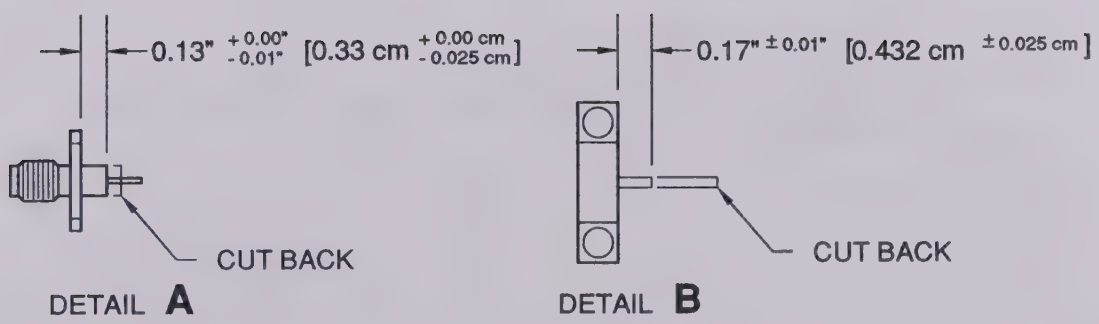
23. Remove connector from Power Termination Assembly (4).

**POWER TERMINATION PC BOARD**

24. Remove three screws (6).

25. Remove Power Termination PC Board (2).




8821011

Power Termination Assembly Disassembly
Figure 9

STEP PROCEDURE

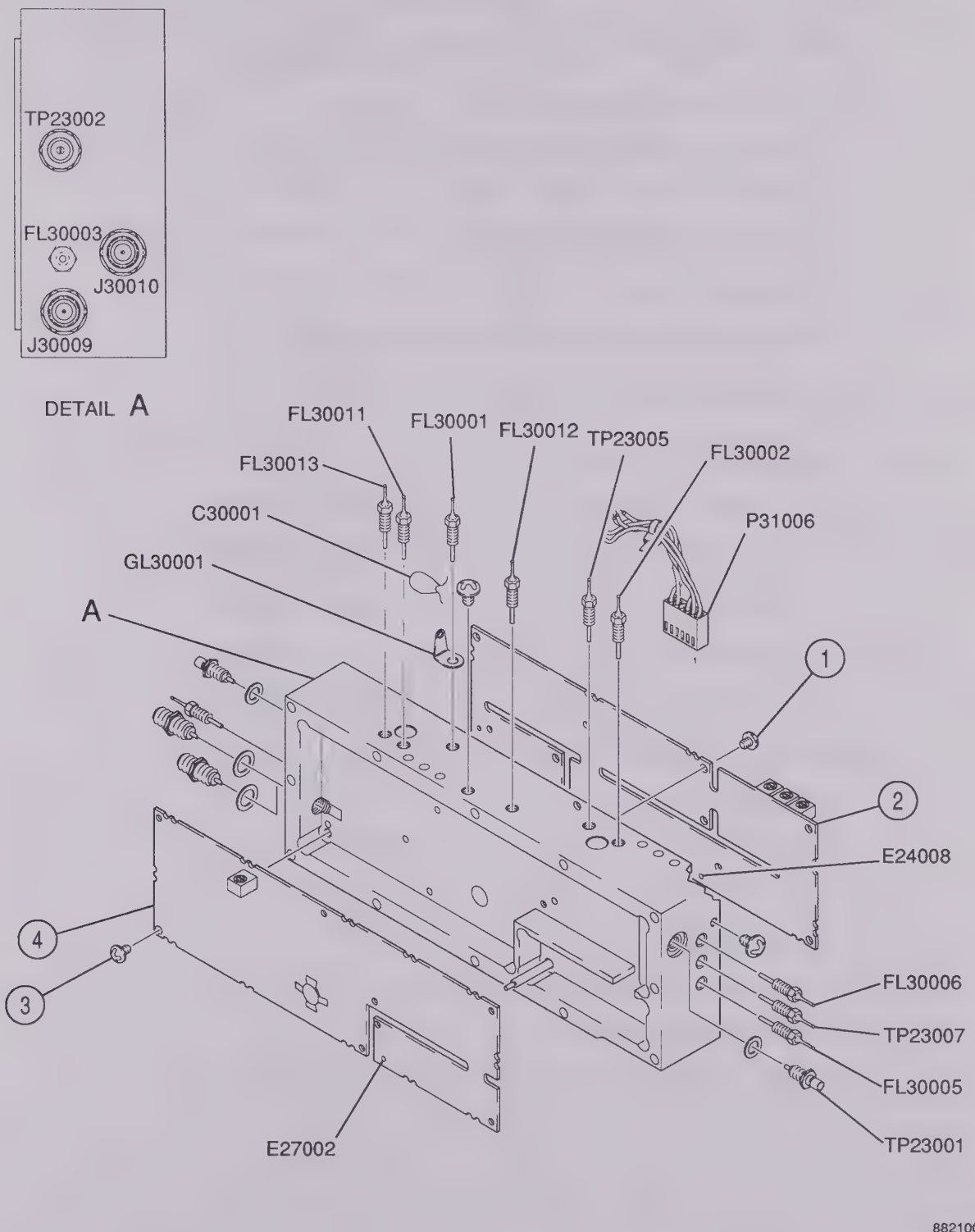
**POWER AMP PC BOARD ASSEMBLY**

**NOTE:** For Steps 26 through 30, refer to 2-3-1, Figure 10.

26. Remove solder and disconnect as follows:
    - Wires (P31006 and FL30002) from FL30013.
    - Wire (P31006) from FL30011.
    - Wires (FL30001 and FL30006) from FL30012.
27. Remove solder from following connections on Power Amp PC Board Assembly (4):
    - FL30012 (E27001)
    - TP23001 (E27008)
    - E27002
    - J30010 (E27003)
    - FL30013 (E27005)
    - FL30011 (E27004)
28. Remove following items from Source/Pwr Amp Assembly:
    - FL30013
    - FL30011
    - FL30012
    - TP23001
    - J30010
29. Remove eight screws (3).
30. Remove Power Amp PC Board Assembly (4).

**1030 MHz SOURCE PC BOARD ASSEMBLY**

31. If MLD is not installed, remove twelve screws (10). If MLD is installed, remove nine screws (10).
32. Remove 1030 MHz Source cover (12).
33. Disconnect P30009 (U23001) from J30009 (Source/Pwr Amp Assembly).




Source/Pwr Amp Assembly Disassembly
Figure 10

STEP PROCEDURE

**NOTE:** For Steps 34 through 38, refer to 2-3-1, Figure 10.

34. Remove solder and disconnect as follows:
    - Wire (FL30003) from FL30005.
    - Wire (FL30012) from FL30006.
    - Wire (FL30013) from FL30002.
    - Wire (P31006) from GL30001.
    - Wires (P31006 and FL30012) from FL30001.
    - Wires (P31006 and FL30005) from FL30003.
35. Remove solder from following connections on 1030 MHz Source PC Board Assembly (2):
    - FL30001 (E24002)
    - TP230002 (E24004)
    - FL30003 (E24001)
    - J30009 (E24003)
    - E24008
    - FL3005 (E24006)
    - TP23007 (E24005)
    - FL30006 (E24007)
    - FL30002 (E24009)
    - TP23005 (E24010)
36. Remove following items from Source/Pwr Amp Assembly:
    - FL30005
    - TP23007
    - FL30006
    - FL30002
    - TP23005
    - TP23002
    - FL30003
    - J30009
    - FL30001/GL30001 (carefully to not twist C30001)
37. Remove nine screws (1).
38. Remove 1030 MHz Source PC Board Assembly (2).

(7) Motherboard PC Board Assembly

**NOTE:** Refer to 2-3-1, Figure 1 (w/o MLD) or Figure 2 (w/ MLD) unless otherwise noted.

| STEP | PROCEDURE |
|---|---|

1. Remove Processor and Pulse PC Board Assemblies according to 2-3-1C(4).

2. Remove Diversity Module according to 2-3-1C(6).

3. Disconnect cables as follows:

   - P20003 (Diversity Module) from J20003 (Motherboard PC Board Assembly).
   - P20004 (Diversity Module) from J20004 (Motherboard PC Board Assembly).
   - P20001 (Power Supply Assembly) from J20001 (Motherboard PC Board Assembly).
   - P15001 (Motherboard PC Board Assembly) from J15001 (Front Panel Assembly). Push tabs out to disconnect.

4. Remove two screws (7).

5. Remove three screws (9), one through J11001 towards center of Motherboard PC Board Assembly (8), one through J20002 in upper outside corner and one in lower outside corner.

6. Remove Motherboard PC Board Assembly (8) from Chassis Assembly (22).

(8) Attenuator Assembly (w/ MLD)

Refer to 2-3-1, Figure 2 (w/ MLD), unless otherwise noted.

| STEP | PROCEDURE |
|---|---|

1. Remove top cover according to 2-3-1C(1).
2. Disconnect cables as follows:
   - P21002 (Diversity Module) from J21002 (Attenuator Assembly).
   - P21003 (Diversity Module) from J21003 (Attenuator Assembly).
   - P21005 (Front Panel Assembly) from J21005 (Attenuator Assembly).
   - P21001 (Front Panel Assembly) from J21001 (Attenuator Assembly).
3. Remove two screws (29).
4. Remove Attenuator Assembly (28).

**ATTENUATOR DRIVER PC BOARD ASSEMBLY**

**NOTE:** For Steps 5 through 14, refer to 2-3-1, Figure 11.

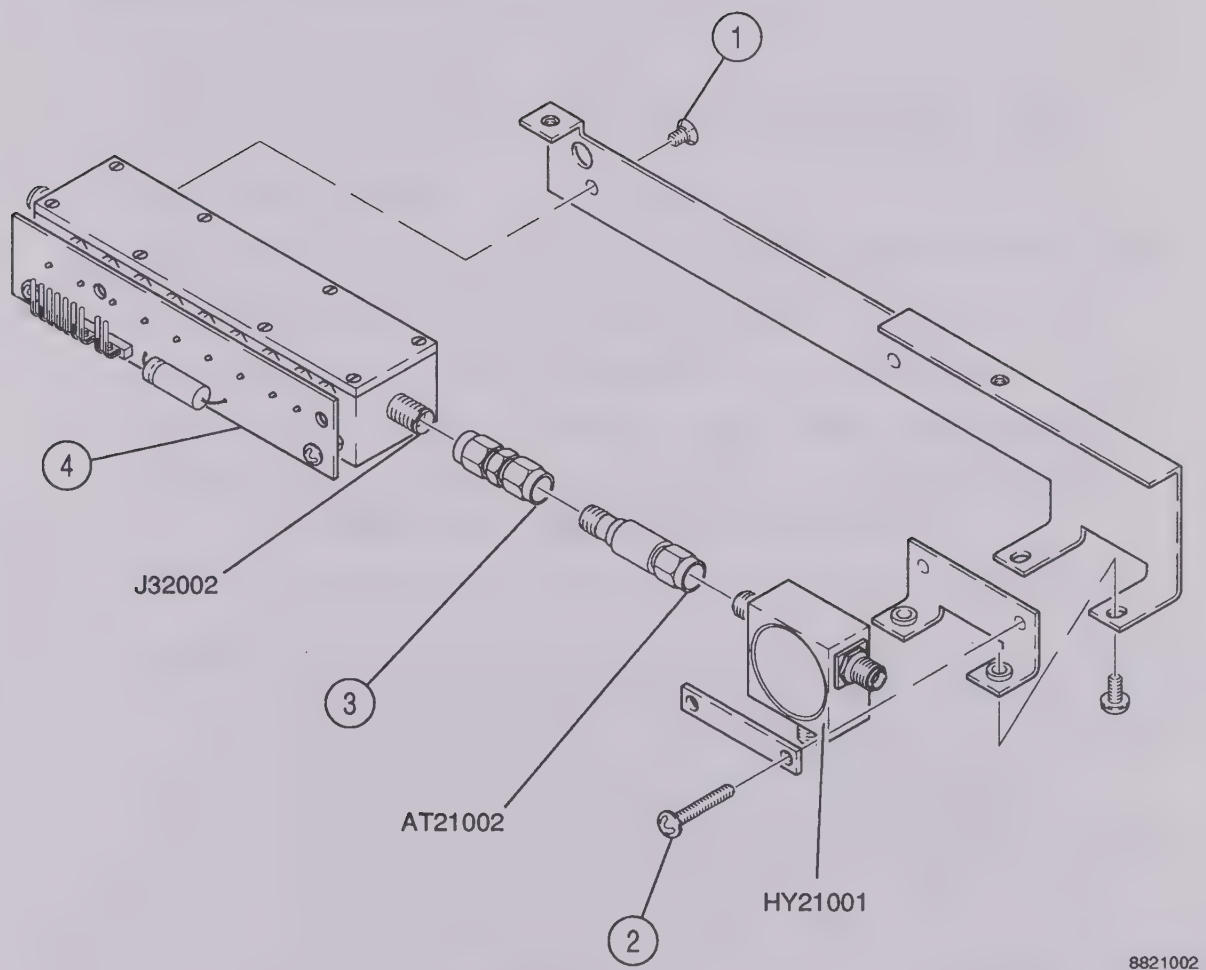
5. Remove two screws (1).
6. Disconnect Adaptor (3) from J32002.
7. Remove Attenuator Driver PC Board Assembly (4).

**ATTENUATOR AT21002**

8. Remove Adaptor (3) from AT21002.
9. Disconnect and remove AT21002 from HY21001.

**CIRCULATOR HY21001**

10. Loosen two screws (2).
11. Remove HY21001.




Attenuator Assembly Disassembly
Figure 11

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## 2. Reassembly

### A. General

Reassembly depends upon extent of disassembly and should be performed with normal repair and/or cleaning. Perform reassembly in reverse sequence of disassembly procedures. Incorporate Special Reassembly Procedures in 2-3-2C as required.

### B. Preliminary Considerations

#### (1) Tools Required

Reassembly requires the same tools required for disassembly. Refer to 2-3-1B(1).

#### (2) Reassembly Precautions

**CAUTION:** INSURE ALL COAXIAL CONNECTIONS ARE PROPERLY MATED.

**CAUTION:** DO NOT BEND OR TWIST SEMI-RIGID COAXIAL CABLES.

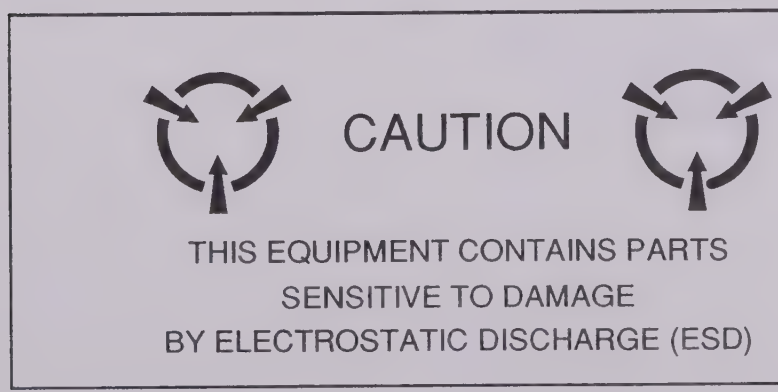
**CAUTION:** ALL RIBBON CABLES MUST LIE FLAT AND NEATLY FOLDED.

**CAUTION:** DO NOT PLACE UNDUE STRAIN ON ANY WIRE OR CABLE.

**CAUTION:** DO NOT OVER TIGHTEN SCREWS AND NUTS INCLUDING COAXIAL CONNECTORS.

**CAUTION:** DO NOT EXPOSE COMPONENTS TO EXCESSIVE HEAT WHEN APPLYING SOLDER.

**CAUTION:** THE ATTENUATOR DRIVER PC BOARD ASSEMBLY (ONLY WITH MLD), DIVERSITY MODULE, FRONT PANEL ASSEMBLY, FRONT PANEL PROCESSOR PC BOARD ASSEMBLY, POWER SUPPLY PC BOARD ASSEMBLY, PROCESSOR PC BOARD ASSEMBLY AND PULSE PC BOARD ASSEMBLY CONTAIN PARTS SENSITIVE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD). ALL PERSONNEL PERFORMING REASSEMBLY SHOULD HAVE KNOWLEDGE OF ACCEPTED ESD PRACTICES.



C. Special Reassembly Procedures

**CAUTION:** REPLACE WORN SHOULDER WASHERS AND INSULATORS. CAREFULLY REINSTALL SHOULDER WASHERS AND INSULATORS IN CORRECT POSITIONS. FAILURE TO INSTALL SHOULDER WASHERS AND INSULATORS CORRECTLY COULD RESULT IN A SHORT CIRCUIT.

(1) Chassis Assembly

None required.

(2) Power Supply Assembly

None required.

(3) Line Supply PC Board Assembly

None required.

(4) Processor and Pulse PC Board Assemblies

None required.

(5) Front Panel Assembly

None required.

(6) Diversity Module

**POWER TERMINATION ASSEMBLY**

- If R28002 is replaced, modify new R28002 according to Detail B of 2-3-1, Figure 9.
- If a connector is replaced, modify new connector according to Detail A of 2-3-1, Figure 9.

(7) Motherboard PC Board Assembly

None required.

(8) Attenuator Assembly

None required.

# APPENDIX A - CONNECTOR PIN-OUT TABLES

1. Table of S-1403C I/O Connectors

| CONNECTOR | SIGNAL NAME | SIGNAL TYPE | INPUT/OUTPUT |
|---|---|---|---|
| FRONT PANEL | | | |
| J10001 | UUT XMTR | 50 Ω | OUTPUT |
| J10002 | ANT B | 50 Ω | INPUT/OUTPUT |
| PULSE PC BOARD ASSEMBLY | | | |
| J10003 | EXT MOD | TTL | INPUT |
| J10004 | EXT SYNC | TTL | INPUT |
| J10005 | ATCRBS DISC | TTL | OUTPUT |
| J10006 | BVIDEO | TTL | OUTPUT |
| J10007 | SCOPE TRIG | TTL | OUTPUT |
| J10008 | EXT SYNC | TTL | OUTPUT |
| J10009 | PREPULSE | TTL | OUTPUT |
| J10010 | AUXILIARY | VARIOUS | INPUT/OUTPUT |
| J10013 | RF VERNIER | 0 TO 7 Vdc | OUTPUT |
| J10014 | MEASURE GATE | TTL | OUTPUT |
| J10015 | DPSK | BIPOLAR | OUTPUT |
| PROCESSOR PC BOARD ASSEMBLY | | | |
| J10011 | IFR BUS | TTL | INPUT/OUTPUT |
| J10012 | TEST | RS-232C | INPUT/OUTPUT |

2. S-1403C AUXILIARY Connector (J10010) Pin-Out Table

| PIN NO. | SIGNAL NAME | SIGNAL TYPE | INPUT/OUTPUT | POLARITY |
|---|---|---|---|---|
| 1 | GROUND | | | |
| 2 | SPARE | | | |
| 3 | SPARE | | | |
| 4 | SPARE | | | |
| 5 | EXTPULSE | TTL | OUTPUT | ACTIVE LOW |
| 6 | EXT SLS | TTL | OUTPUT | ACTIVE LOW |
| 7 | SPARE | | | |
| 8 | PULSE | TTL | INPUT | POSITIVE |
| 9 | 20 MHz | TTL | INPUT | RISING EDGE |
| 10 | SPARE | | | |
| 11 | 50% VIDEO | TTL | INPUT | POSITIVE |
| 12 | SPARE | | | |
| 13 | SPARE | | | |
| 14 | SELF INTERROGATE | TRISTATE | INPUT/OUTPUT | RISING EDGE |
| 15 | GROUND | | | |
| 16 | GROUND | | | |
| 17 | GROUND | | | |
| 18 | GROUND | | | |
| 19 | GROUND | | | |
| 20 | GROUND | | | |
| 21 | GROUND | | | |
| 22 | GROUND | | | |
| 23 | SPARE | | | |
| 24 | GROUND | | | |
| 25 | SPARE | | | |

3. S-1403C IFR BUS Connector (J10011) Pin-Out Table

| PIN NO. | SIGNAL NAME | SIGNAL TYPE | INPUT/OUTPUT | POLARITY |
|---|---|---|---|---|
| 1 | GROUND | | | |
| 2 | A0 | TTL | INPUT | POSITIVE |
| 3 | A1 | TTL | INPUT | POSITIVE |
| 4 | GROUND | | | |
| 5 | A2 | TTL | INPUT | POSITIVE |
| 6 | D7 | TTL | INPUT/OUTPUT | POSITIVE |
| 7 | D6 | TTL | INPUT/OUTPUT | POSITIVE |
| 8 | A3 | TTL | INPUT | POSITIVE |
| 9 | GROUND | | | |
| 10 | GROUND | | | |
| 11 | NOT USED | | | |
| 12 | D5 | TTL | INPUT/OUTPUT | POSITIVE |
| 13 | GROUND | | | |
| 14 | NOT USED | | | |
| 15 | D4 | TTL | INPUT/OUTPUT | POSITIVE |
| 16 | GROUND | | | |
| 17 | WRITE | TTL | INPUT | POS STROBE |
| 18 | D3 | TTL | INPUT/OUTPUT | POSITIVE |
| 19 | GROUND | | | |
| 20 | READ | TTL | INPUT | POS STROBE |
| 21 | D2 | TTL | INPUT/OUTPUT | POSITIVE |
| 22 | INTA | OC | OUTPUT | ACTIVE LOW |
| 23 | INTR | OC | INPUT | ACTIVE |
| 24 | D1 | TTL | INPUT/OUTPUT | POSITIVE |
| 25 | D0 | TTL | INPUT/OUTPUT | POSITIVE |

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# APPENDIX B - ABBREVIATIONS

## A

| | |
|---|---|
| A | Amperes |
| AA | Address Announced |
| AC | Altitude Code |
| AC | Alternating Current |
| ac | Alternating Current |
| ACAS | Airborne Collision Avoidance System |
| ACL | All-Call Long |
| ACS | All-Call Short |
| A/D | Analog-to-Digital |
| ADD | Address |
| ADS | A-Definition Subfield |
| ALC | Automatic Level Control |
| AM | Amplitude Modulation |
| AMPL | Amplifier |
| ANT | Antenna |
| Ant | Antenna |
| AP | Address Parity |
| APER | Ant A Percent Reply for ATCRBS |
| AQ | Acquisition Special |
| ASCII | American Standard Code for Information Interchange |
| AT | Attenuator |
| ATC | ATCRBS |
| ATCRBS | Air Traffic Control Radar Beacon System |
| ATE | Automatic Test Equipment |
| ATIS | Automated Terminal Information System |
| AUX | Auxiliary |

## B

| | |
|---|---|
| BDS | B-Definition Subfield |
| BN | BURST Number |
| BPER | Ant B Percent Reply |
| BPF | Bandpass Filter |
| BPulse | Diversity Pulse |
| BRF | RF through Ant B |
| Brf | RF through Ant B |
| BRFLV | RF level through Ant B |
| Brflvl | RF level through Ant B |
| BT | Battery |
| BVideo | Antenna B Diversity Video |

## C

| | |
|---|---|
| C | Capacitor |
| C | Centigrade |
| CA | Capability |
| CAL | Calibrated Position |
| ccw | Counterclockwise |
| CFS | Continuation Subfield |
| CHAN | Channel |
| cm | Centimeter ($10^{-2}$) |
| CMENU | Control Menu |
| COMP | Compensator |
| Cont | Continued |
| CR | Diode |
| CW | Continuous Wave |
| cw | Clockwise |

## D

| | |
|---|---|
| DABS | Discrete Address Beacon System |
| DAC | Digital-to-Analog |
| dB | Decibel |
| dc | Direct Current |
| DBL | Double |
| dBm | Decibels compared to 1 milliwatt |
| DET | Detector |
| DEV | Deviation |
| DF | Downlink Format |
| DFSQnn | Downlink Format Sequence Number |
| DI | Designator Identification |
| DI | Double Interrogation |
| DISC | Discrete |
| DIV | Diversity |
| DMA | Direct Memory Access |
| DME | Distance Measuring Equipment |
| DMM | Digital Multimeter |
| DO | Document |
| DPSK | Differential Phase Shift Keying |
| DR | Downlink Request |
| DRVR | Driver |
| DS | Display or LED |
| Dv | Deviation |

**E**

| | |
|---|---|
| ECL | Extended Command Language |
| ECS | Extended Capability Subfield |
| ELM | Extended Length Message |
| ENT | Enter |
| ERRM | Error Message |
| ESC | Escape |
| ESD | Electrostatic Discharge |
| EXMOD | External Modulation |
| EXSYN | External Synchronization |
| EXT | External |
| Ext | External |

**F**

| | |
|---|---|
| FL | Feed Through Filter |
| FMT | Format |
| FP | Front Panel |
| FPM | Feet Per Minute |
| FREQ | Frequency |
| FS | Flight Status |
| FUNC | Function |
| Fun | Function |
| FUN NO | Function Number |
| F/W | Firmware |

**G**

| | |
|---|---|
| GEN | Generator |
| GHz | Gigahertz ($10^9$) |
| GND | Ground |
| GPIB | General Purpose Interface Bus |

**H**

| | |
|---|---|
| h | Hexadecimal |
| HET | Heterodyne |
| HY | Hybrid (Coupler, Circulator, etc.) |
| Hz | Hertz |

**I**

| | |
|---|---|
| IC | Integrated Circuit |
| ID | Identification (4906 Code) |
| IEEE | Institute of Electrical and Electronics Engineers |
| IDS | Identifier Designators Subfield |
| IF | Intermediate Frequency |
| IFR | IFR Systems, Inc |
| II | Interrogator Identification |
| IIS | Interrogator Identification Subfield |
| IN | Input |
| INTRF | Interference |
| INTERR | Interrogation |
| INTERRF | Interference |
| INTLCE | Interlace |
| I/O | Input/Output |

**J**

| | |
|---|---|
| J | Jack Connector |

**K**

| | |
|---|---|
| KE | Control, ELM |
| kg | Kilogram ($10^3$) |
| kHz | Kilohertz ($10^3$) |
| kts | Knots (Velocity) |

**L**

| | |
|---|---|
| L | Inductor |
| LCA | Logic Cell Array |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| LO | Local Oscillator |
| LOS | Lockout Subfield |
| LPF | Low-Pass Filter |
| LVL | Level |

**M**

| | |
|---|---|
| MA | Message, COMM-A |
| MAN | Manual |
| MAX | Maximum |
| MB | Message, COMM-B |
| MBS | Multisite COMM-B Subfield |
| MC | Message, COMM-C |
| MCPU | Main Central Processing Unit |
| MD | Message, COMM-D |
| MECH | Mechanical |
| MES | Multi-site ELM Sub-field |
| MHz | Megahertz ($10^6$) |
| MIN | Minimum |
| MLD | Multi-Level Diversity |
| MOD | Modulator |
| µs | Microsecond ($10^{-6}$) |
| ms | Millisecond ($10^{-3}$) |
| MTL | Minimum Threshold Level |
| MU | Message, COMM-U |
| MUART | Multifunction Universal Asynchronous Receiver-Transmitter |
| MV | Message, COMM-V |
| MX | Mixer |

**N**

| | |
|---|---|
| NA | Not Applicable |
| NC | Number of C-Segment |
| ND | Number of D Segment |
| NO | Number |
| No | Number |
| NOM | Nominal |
| NORM | Normal |
| ns | Nanosecond ($10^{-9}$) |

**O**

| | |
|---|---|
| OC | Open Collector |
| OUT | Output |

**P**

| | |
|---|---|
| P | Plug Connector |
| PC | Protocol |
| PC | Printed Circuit |
| PI | Parity/Interrogator Identity |
| PLL | Phase-Locked Loop |
| PN | Part Number |
| POS | Positive |
| PPG | Pulse Power Gate |
| PPM | Pulse Position Modulation |
| PPMG | Pulse Power Measurement Gate |
| PPULSE | Prepulse |
| PPuls | Prepulse |
| PR | Probability of Reply |
| PRF | Pulse Repetition Frequency |
| PRPLY | Percent Reply |
| PWR | Power |

**Q**

| | |
|---|---|
| Q | Transistor |

**R**

| | |
|---|---|
| R | Resistor |
| RAM | Random Access Memory |
| RCVR | Receiver |
| RE | Rotary Encoder |
| RECALLn | Recall (number) |
| RECT | Rectifier |
| REF | Reference |
| REG | Regulator |
| RF | Radio Frequency |
| RFLV | RF Level |
| RFLvl | RF Level |
| RI | Reply Information, Air-to-Air |
| RL | Reply Length |
| RMS | Root Mean Square |
| RN | Resistive Network |
| ROM | Read Only Memory |
| RPDLY | Reply Delay |
| RpDly | Reply Delay |
| RR | Reply Request |
| RRS | Reply Request Subfield |
| RSS | Reservation Status Subfield |
| RTCA | Radio Technical Commission for Aeronautics |

**S**

| | |
|---|---|
| S | Switch |
| SAVEn | Save (number) |
| SCOPE | Oscilloscope |
| SD | Special Designator |
| sec | second |
| SEQ | Sequence |
| Seq | Sequence |
| SEQn | Sequence Number |
| SLS | Side-Lobe Suppression |
| SMENU | Sequence Menu |
| SPI | Special Identifier Pulse |
| spi | Special Identifier Pulse |
| SPER | Ant A Percent Reply for Mode S |
| SPR | Synchronous Phase Reversal |
| SQADD | Squitter Address |
| SQnn | Sequence Menu (number) |
| SQTR | Squitter |
| Sqtr | Squitter |
| SRQ | Service Request |
| SRS | Segment Request Subfield |
| SSR | Secondary Surveillance Radar |
| SYNC | Synchronous |
| sync | Synchronous |

**T**

| | |
|---|---|
| T | Transformer |
| TAC | TACAN |
| TCAS | Traffic Alert and Collision Avoidance System |
| TCXO | Temperature Compensated Crystal Oscillator |
| TEMP | Temperature |
| TERM | Terminal |
| $T_D$ | Reply Sync |
| TMS | Tactical Message Subfield |
| $T_O$ | Interrogation sync |
| TP | Test Point |
| TRIG | Trigger |
| TTL | Transistor-Transistor Logic |

**U**

| | |
|---|---|
| U | Integrated Circuit Chip |
| UF | Uplink Field |
| UM | Utility Message |
| UUT | Unit Under Test |

**V**

| | |
|---|---|
| V | Volts |
| VAC | Volts Alternating Current |
| VAR | Variation |
| VCO | Voltage Controlled Oscillator |
| VCXO | Voltage-Controlled Crystal Oscillator |
| Vdc | Volts Direct Current |
| VER | Version (firmware) |
| $V_{P-P}$ | Volts Peak-to-Peak |
| VRAM | Video Random Access Memory |
| Vrms | Volts Root Mean Square |
| VS | Vertical Status |

**W**

| | |
|---|---|
| w/ | With |
| W | Watts |
| Wd | Width |
| w/o | Without |

**X**

| | |
|---|---|
| XMTR | Transmitter |
| XPDR | Transponder |

**Y**

| | |
|---|---|
| Y | Crystal |

# APPENDIX C - TEST EQUIPMENT REQUIREMENTS

## 1. General

This Appendix contains a list of test equipment suitable for performing all of the maintenance procedures contained in this manual. Other equipment meeting the specifications listed in this Appendix may be substituted in place of the recommended models. The equipment listed in this Appendix may exceed the minimum required specifications for some of the procedures contained in this manual.

## 2. Recommended Test Equipment

| TYPE | MODEL | SPECIFICATIONS |
|---|---|---|
| 10 dB Attenuator | HP8491A<br>or Equivalent | Frequency Range:<br>dc to 12.4 GHz |
| Digital Multimeter | FLUKE 8010A<br>or Equivalent | ±50.00 Vdc Range<br>5.5 Digit<br>±0.1% Basic dc Accuracy |
| Dual Pulse Generator | WAVETEK 145<br>or Equivalent | Functions:<br>Pulse<br>Pulse Delay:<br>50 ns to 10 ms<br>Pulse Width:<br>25 ns to 1 ms<br>Output Level:<br>15 Vp-p into 50 Ω |
| Frequency Counter | FLUKE 7220A<br>or Equivalent | Frequency Range:<br>10 Hz to 1300 MHz<br>Resolution:<br>10 Hz<br>Accuracy:<br>±1 Count (±Time Base Error) |
| Heterodyne Monitor | ANZAC MD-141<br>or Equivalent | |

| TYPE | MODEL | SPECIFICATIONS |
|---|---|---|
| Oscilloscope | TEK 2465<br>or Equivalent | Bandwidth:<br>dc to 100 MHz<br>Vertical Accuracy:<br>±10%<br>Time Accuracy:<br>±0.7% of Time Interval<br>±0.6% of Full Scale<br>Δ Time Accuracy:<br>±0.7% of Time Interval<br>±0.3% of Full Scale |
| Power Meter | BOONTON 4200<br>(with Power Sensor)<br>or Equivalent | Range:<br>-25 to -15 dBm<br>Accuracy:<br>±0.05 dB |
| RF Signal Generator | HP8640B<br>or Equivalent | Frequency Range:<br>1 to 1030 MHz<br>Resolution:<br>0.1 to 100 Hz<br>Accuracy:<br>$2 \times 10^{-6}$<br>RF Output:<br>13 to -130 dBm |
| Spectrum Analyzer | HP8569B<br>or Equivalent | Frequency Range:<br>10 kHz to 2.6 GHz<br>Resolution Bandwidth:<br>300 Hz to 3.0 MHz<br>Display Accuracy Log:<br><±0.1 dB/dB<br><±1.5 dB/70 dB<br>Display Accuracy Linear:<br><±3% of reference level<br>over full 8 division deflection |

# APPENDIX D - METRIC/BRITISH IMPERIAL CONVERSION TABLE WITH NAUTICAL DISTANCE CONVERSIONS

| TO CONVERT: | INTO: | MULTIPLY BY: | TO CONVERT: | INTO: | MULTIPLY BY: |
|---|---|---|---|---|---|
| cm | feet | 0.03281 | meters | feet | 3.281 |
| cm | inches | 0.3937 | meters | inches | 39.37 |
| feet | cm | 30.48 | m/sec | ft/sec | 3.281 |
| feet | meters | 0.3048 | m/sec | km/hr | 3.6 |
| ft/sec | km | 1.097 | m/sec | miles/hr | 2.237 |
| ft/sec | knots | 0.5921 | miles | feet | 5280 |
| ft/sec | miles/hr | 0.6818 | miles | km | 1.609 |
| $ft/sec^2$ | $cm/sec^2$ | 30.48 | miles | meters | 1609 |
| $ft/sec^2$ | $m/sec^2$ | 0.3048 | miles | nmi | 0.8684 |
| grams | ounces | 0.03527 | miles/hr | ft/sec | 1.467 |
| inches | cm | 2.54 | miles/hr | km/hr | 1.609 |
| kg | pounds | 2.205 | miles/hr | knots | 0.8684 |
| $kg/cm^2$ | psi | 0.0703 | nmi | feet | 6080.27 |
| km | feet | 3281 | nmi | km | 1.8532 |
| km | miles | 0.6214 | nmi | meters | 1853.2 |
| km | nmi | 0.5396 | nmi | miles | 1.1516 |
| km/hr | ft/sec | 0.9113 | ounces | grams | 28.34953 |
| km/hr | knots | 0.5396 | pounds | kg | 0.4536 |
| km/hr | miles/hr | 0.6214 | psi | $kg/cm^2$ | 0.0703 |
| knots | ft/sec | 1.689 | 100 ft | km | 3.048 |
| knots | km/hr | 1.8532 | 100 ft | miles | 1.894 |
| knots | miles/hr | 1.1516 | 100 ft | nmi | 1.645 |

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# INDEX


| Title | Chapter/Section/Subject | Page |
|---|---|---|
| 10 MHz TCXO | | |
| Disassembly | 2-3-1 | 20 |
| Theory of Operation | 2-2-1 | 36 |
| 1030 MHz Source PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 22 |
| Block Diagram | 2-2-1 | 36 |
| Circuit Schematic | 2-2-3 | 23 |
| Disassembly | 2-3-1 | 24 |
| Theory of Operation | 2-2-1 | 36 |
| Abbreviations | Appendix B | 1 |
| Attenuator Assembly | | |
| Assembly Drawing | 2-2-3 | 28 |
| Block Diagram | 2-2-1 | 45 |
| Circuit Schematic | 2-2-3 | 28 |
| Disassembly | 2-3-1 | 28 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 45 |
| Attenuator Driver PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 28 |
| Block Diagram | 2-2-1 | 45 |
| Circuit Schematic | 2-2-3 | 28 |
| Disassembly | 2-3-1 | 28 |
| Theory of Operation | 2-2-1 | 45 |
| Basic System Protocol | 2-2-1 | 1 |
| Calibration/Verification | 2-2-2 | 1 |
| Data Sheet | 2-2-2 | 26 |
| Procedures | 2-2-2 | 5 |
| Antenna B | 2-2-2 | 18 |
| Interrrogation Pulses and SPR | 2-2-2 | 7 |
| Power Supply | 2-2-2 | 5 |
| Reply Delay and PPMG | 2-2-2 | 22 |
| RF Level | 2-2-2 | 16 |
| Suppressor and Interference Pulses | 2-2-2 | 13 |
| Chassis Assembly | | |
| Disassembly | 2-3-1 | 5 |
| Reassembly | 2-3-2 | 2 |
| Communications, S-1403C to ATC-1400A | 2-2-1 | 3 |
| Composite Assembly (w/ MLD) | | |
| Assembly Drawing | 2-2-3 | 4 |
| Interconnect Diagram | 2-2-3 | 4 |
| Composite Assembly (w/o MLD) | | |
| Assembly Drawing | 2-2-3 | 3 |
| Interconnect Diagram | 2-2-3 | 3 |
| Disassembly | 2-3-1 | 1 |
| Disassembly Procedures | 2-3-1 | 5 |
| Attenuator Assembly (with MLD) | 2-3-1 | 28 |
| Attenuator AT21002 | 2-3-1 | 28 |
| Attenuator Driver PC Board Assembly | 2-3-1 | 28 |
| Circulator HY21001 | 2-3-1 | 28 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Disassembly Procedures (Cont) | | |
| Chassis Assembly | 2-3-1 | 5 |
| Fan | 2-3-1 | 5 |
| Side Rails | 2-3-1 | 5 |
| Top Cover | 2-3-1 | 5 |
| Diversity Module | 2-3-1 | 14 |
| Modulator Assembly | 2-3-1 | 14 |
| Diversity I/O PC Board Assembly | 2-3-1 | 17 |
| Modulator PC Board Assembly | 2-3-1 | 18 |
| Video Filter PC Board Assembly | 2-3-1 | 17 |
| Source/Pwr Amp Assembly | 2-3-1 | 20 |
| 10 MHz TCXO (U23001) | 2-3-1 | 20 |
| 1030 MHz PC Board Assembly | 2-3-1 | 24 |
| Connectors J28029 and J23014 | 2-3-1 | 22 |
| Power Amp PC Board Assembly | 2-3-1 | 24 |
| Power Termination Assembly (w/ MLD) | 2-3-1 | 20 |
| Power Termination Assembly (w/o MLD) | 2-3-1 | 20 |
| Power Termination PC Board | 2-3-1 | 22 |
| Resistor R28002 | 2-3-1 | 22 |
| Video Detector PC Board Assembly (with MLD) | 2-3-1 | 21 |
| Front Panel Assembly | 2-3-1 | 11 |
| Front Panel Processor PC Board Assembly | 2-3-1 | 12 |
| Keyboard PC Board Assembly | 2-3-1 | 12 |
| Menu Display | 2-3-1 | 12 |
| Line Supply PC Board Assembly | 2-3-1 | 9 |
| Motherboard PC Board Assembly | 2-3-1 | 27 |
| Power Supply Assembly | 2-3-1 | 5 |
| Filters | 2-3-1 | 9 |
| Inverter Supply PC Board Assembly | 2-3-1 | 6 |
| Power Distribution PC Board Assembly | 2-3-1 | 6 |
| Processor and Pulse PC Board Assemblies | 2-3-1 | 10 |
| Disassembly/Reassembly | 2-3 | 1 |
| Diversity Module | | |
| Assembly Drawing (w/ MLD) | 2-2-3 | 20 |
| Assembly Drawing (w/o MLD) | 2-2-3 | 19 |
| Block Diagram | 2-2-1 | 35 |
| Disassembly | 2-3-1 | 14 |
| Interconnect Diagram (w/ MLD) | 2-2-3 | 20 |
| Interconnect Diagram (w/o MLD) | 2-2-3 | 19 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 34 |
| Diversity I/O PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 24 |
| Block Diagram | 2-2-1 | 39, 40 |
| Circuit Schematic | 2-2-3 | 25, 27 |
| Disassembly | 2-3-1 | 17 |
| Theory of Operation | 2-2-1 | 38 |
| External Cleaning | 2-1-1 | 1 |
| Fan Disassembly | 2-3-1 | 5 |
| Front Panel Assembly | | |
| Assembly Drawing | 2-2-3 | 10 |
| Block Diagram | 2-2-3 | 18 |
| Disassembly | 2-3-1 | 11 |
| Interconnect Diagram | 2-3-1 | 10 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 18 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Front Panel Processor PC Board Assembly | | |
| Assembly Drawing (w/ MLD) | 2-2-3 | 14 |
| Assembly Drawing (w/o MLD) | 2-2-3 | 12 |
| Block Diagram | 2-2-3 | 18 |
| Circuit Schematic (w/ MLD) | 2-2-3 | 15 |
| Circuit Schematic (w/o MLD) | 2-2-3 | 13 |
| Disassembly | 2-3-1 | 12 |
| Theory of Operation | 2-2-1 | 19 |
| Functional Theory of Operation | 2-2-1 | 4 |
| Introduction | 2-2-1 | 4 |
| Receive | 2-2-1 | 5 |
| Test Validity | 2-2-1 | 7 |
| Transmit | 2-2-1 | 6 |
| Interface, Mode S Test System S-1403C to ATC-1400A | | |
| Definition | 2-2-1 | 3 |
| Operation | 2-2-1 | 4 |
| Internal Cleaning | 2-1-1 | 1 |
| Inverter Supply PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 6 |
| Block Diagram | 2-2-1 | 9 |
| Circuit Schematic | 2-2-3 | 7 |
| Disassembly | 2-3-1 | 6 |
| Theory of Operation | 2-2-1 | 8 |
| I/O Connectors and Pin-Out Tables | Appendix A | 1 |
| Keyboard PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 11 |
| Circuit Schematic | 2-2-3 | 11 |
| Disassembly | 2-3-1 | 12 |
| Theory of Operation | 2-2-1 | 19 |
| Line Supply PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 5 |
| Block Diagram | 2-2-1 | 7 |
| Circuit Schematic | 2-2-3 | 5 |
| Disassembly | 2-3-1 | 9 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 7 |
| Major Operating Characteristics | 2-2-1 | 1 |
| Menu Display | | |
| Disassembly | 2-3-1 | 12 |
| Theory of Operation | 2-2-1 | 21 |
| Metric/British Imperial Conversion Table with Nautical Distance Conversions | Appendix D | 1 |
| Mode S Function | 2-2-1 | 1 |
| Mode S Message Content | 2-2-1 | 2 |
| Mode S Test System S-1403C to ATC-1400A Interface | | |
| Definition | 2-2-1 | 3 |
| Operation | 2-2-1 | 4 |
| Modulator Assembly (w/ MLD) | | |
| Assembly Drawing | 2-2-3 | 26 |
| Block Diagram | 2-2-1 | 40 |
| Circuit Schematic | 2-2-3 | 27 |
| Disassembly | 2-3-1 | 14 |
| Theory of Operation | 2-2-1 | 38 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Modulator Assembly (w/o MLD) | | |
| Assembly Drawing | 2-2-3 | 24 |
| Block Diagram | 2-2-1 | 39 |
| Circuit Schematic | 2-2-3 | 25 |
| Disassembly | 2-3-1 | 14 |
| Theory of Operation | 2-2-1 | 38 |
| Modulator PC Board Assembly (w/ MLD) | | |
| Assembly Drawing | 2-2-3 | 26 |
| Block Diagram | 2-2-1 | 40 |
| Circuit Schematic | 2-2-3 | 27 |
| Disassembly | 2-3-1 | 18 |
| Theory of Operation | 2-2-1 | 42 |
| Modulator PC Board Assembly (w/o MLD) | | |
| Assembly Drawing | 2-2-3 | 24 |
| Block Diagram | 2-2-1 | 39 |
| Circuit Schematic | 2-2-3 | 25 |
| Disassembly | 2-3-1 | 18 |
| Theory of Operation | 2-2-1 | 42 |
| Module Theory of Operation | 2-2-1 | 7 |
| Attenuator Assembly | 2-2-1 | 45 |
| Diversity Module | 2-2-1 | 34 |
| 10 MHz TCXO | 2-2-1 | 36 |
| 1030 MHz Source PC Board Assembly | 2-2-1 | 36 |
| Diversity I/O PC Board Assembly | 2-2-1 | 38 |
| Modulator PC Board Assembly | 2-2-1 | 42 |
| Power Amp PC Board Assembly | 2-2-1 | 37 |
| Power Termination Assembly | 2-2-1 | 43 |
| Video Detector PC Board Assembly (only with MLD) | 2-2-1 | 44 |
| Video Filter PC Board Assembly | 2-2-1 | 44 |
| Front Panel Assembly | 2-2-1 | 18 |
| Antenna B Level Control (only with MLD) | 2-2-1 | 23 |
| Keyboard | 2-2-1 | 19 |
| LCD Interface | 2-2-1 | 21 |
| Processor/Memory | 2-2-1 | 22 |
| Slew Controller | 2-2-1 | 19 |
| Power Supply | 2-2-1 | 7 |
| Inverter Supply PC Board Assembly | 2-2-1 | 8 |
| Line Supply Assembly | 2-2-1 | 7 |
| Power Distribution PC Board Assembly | 2-2-1 | 10 |
| Processor PC Board Assembly | 2-2-1 | 11 |
| Analog to Digital Converter | 2-2-1 | 16 |
| Front Panel Interface | 2-2-1 | 17 |
| Processor/System Memory | 2-2-1 | 12 |
| Pulse PC Board Interface | 2-2-1 | 17 |
| Serial/Parallel I/O | 2-2-1 | 14 |
| Pulse PC Board Assembly | 2-2-1 | 24 |
| Control | 2-2-1 | 32 |
| Edge Detect | 2-2-1 | 29 |
| Pulse Generator | 2-2-1 | 26 |
| Reply Decoder | 2-2-1 | 31 |
| RF Vernier | 2-2-1 | 33 |
| Motherboard PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 18 |
| Circuit Schematic | 2-2-3 | 18 |
| Disassembly | 2-3-1 | 27 |
| Reassembly | 2-3-2 | 2 |
| Operating Characteristics, Major | 2-2-1 | 1 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| PC Boards and Schematics | 2-2-3 | 1 |
| Attenuator Assembly | 2-2-3 | 28 |
| Attenuator Driver PC Board Assembly | 2-2-3 | 28 |
| Circuit Schematic | 2-2-3 | 28 |
| Composite Assembly (w/ MLD) | 2-2-3 | 4 |
| Interconnect Diagram | 2-2-3 | 4 |
| Composite Assembly (w/o MLD) | 2-2-3 | 3 |
| Interconnect Diagram (w/o MLD) | 2-2-3 | 3 |
| Diversity Module (w/ MLD) | 2-2-3 | 20 |
| Interconnect Diagram | 2-2-3 | 20 |
| Modulator Assembly | 2-2-3 | 26 |
| Circuit Schematic | 2-2-3 | 27 |
| Diversity I/O PC Board Assembly | 2-2-3 | 24 |
| Modulator PC Board Assembly | 2-2-3 | 26 |
| Video Filter PC Board Assembly | 2-2-3 | 24 |
| Power Termination Assembly | 2-2-3 | 21 |
| Circuit Schematic | 2-2-3 | 21 |
| Power Termination PC Board | 2-2-3 | 21 |
| Source/Pwr Amp Assembly | 2-2-3 | 22 |
| 1030 MHz Source PC Board Assembly | 2-2-3 | 22 |
| Circuit Schematic | 2-2-3 | 23 |
| Power Amp PC Board Assembly | 2-2-3 | 22 |
| Video Detector Assembly | 2-2-3 | 21 |
| Circuit Schematic | 2-2-3 | 21 |
| Diversity Module (w/o MLD) | 2-2-3 | 19 |
| Interconnect Diagram | 2-2-3 | 19 |
| Modulator Assembly | 2-2-3 | 24 |
| Circuit Schematic | 2-2-3 | 25 |
| Diversity I/O PC Board Assembly | 2-2-3 | 24 |
| Modulator PC Board Assembly | 2-2-3 | 24 |
| Video Filter PC Board Assembly | 2-2-3 | 24 |
| Power Termination Assembly | 2-2-3 | 21 |
| Circuit Schematic | 2-2-3 | 21 |
| Power Termination PC Board | 2-2-3 | 21 |
| Source/Pwr Amp Assembly | 2-2-3 | 22 |
| 1030 MHz Source PC Board Assembly | 2-2-3 | 22 |
| Circuit Schematic | 2-2-3 | 23 |
| Power Amp PC Board Assembly | 2-2-3 | 22 |
| Front Panel Assembly | 2-2-3 | 10 |
| Front Panel Processor PC Board Assembly (w/ MLD) | 2-2-3 | 14 |
| Circuit Schematic | 2-2-3 | 15 |
| Front Panel Processor PC Board Assembly (w/o MLD) | 2-2-3 | 12 |
| Circuit Schematic | 2-2-3 | 13 |
| Interconnect Diagram | 2-2-3 | 10 |
| Keyboard PC Board Assembly | 2-2-3 | 11 |
| Circuit Schematic | 2-2-3 | 11 |
| Line Supply PC Board Assembly | 2-2-3 | 5 |
| Circuit Schematic | 2-2-3 | 5 |
| Motherboard PC Board Assembly | 2-2-3 | 18 |
| Circuit Schematic | 2-2-3 | 18 |
| Power Supply Assembly | 2-2-3 | 6 |
| Circuit Schematic | 2-2-3 | 7 |
| Inverter Supply PC Board Assembly | 2-2-3 | 6 |
| Power Distribution PC Board Assembly | 2-2-3 | 6 |
| Processor PC Board Assembly | 2-2-3 | 8 |
| Circuit Schematic | 2-2-3 | 9 |
| Pulse PC Board Assembly | 2-2-3 | 16 |
| Circuit Schematic | 2-2-3 | 17 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Power Amp PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 22 |
| Block Diagram | 2-2-1 | 38 |
| Circuit Schematic | 2-2-3 | 23 |
| Disassembly | 2-3-1 | 24 |
| Theory of Operation | 2-2-1 | 37 |
| Power Distribution PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 6 |
| Circuit Schematic | 2-2-3 | 7 |
| Disassembly | 2-3-1 | 6 |
| Theory of Operation | 2-2-1 | 10 |
| Power Supply Assembly | | |
| Assembly Drawing | 2-2-3 | 6 |
| Circuit Schematic | 2-2-3 | 7 |
| Disassembly | 2-3-1 | 5 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 7 |
| Power Termination Assembly | | |
| Assembly Drawing | 2-2-3 | 21 |
| Circuit Schematic | 2-2-3 | 21 |
| Disassembly | 2-3-1 | 22 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 43 |
| Preventive Maintenance Procedures | 2-1-1 | 1 |
| Processor PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 8 |
| Block Diagram | 2-2-1 | 11 |
| Circuit Schematic | 2-2-3 | 9 |
| Disassembly | 2-3-1 | 10 |
| Reassembly | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 11 |
| Pulse PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 16 |
| Block Diagram | 2-2-1 | 25 |
| Circuit Schematic | 2-2-3 | 17 |
| Disassembly | 2-3-1 | 10 |
| Reassemlby | 2-3-2 | 2 |
| Theory of Operation | 2-2-1 | 24 |
| Reassembly | 2-3-2 | 1 |
| Reassembly Procedures | 2-3-2 | 2 |
| Attenuator Assembly | 2-3-2 | 2 |
| Chassis Assembly | 2-3-2 | 2 |
| Front Panel Assembly | 2-3-2 | 2 |
| Line Supply PC Board Assembly | 2-3-2 | 2 |
| Motherboard PC Board Assembly | 2-3-2 | 2 |
| Power Supply Assembly | 2-3-2 | 2 |
| Processor and Pulse PC Board Assemblies | 2-3-2 | 2 |
| Recommended Test Equipment | Appendix C | 1 |
| S-1403C AUXILIARY Connector (J10010) Pin-Out Table | Appendix A | 2 |
| S-1403C IFR BUS Connector (J10011) Pin-Out Table | Appendix A | 3 |
| Servicing 2-1 | | |
| Source/Pwr Amp Assembly | | |
| Assembly Drawing | 2-2-3 | 22 |
| Circuit Schematic | 2-2-3 | 23 |
| Disassembly | 2-3-1 | 20 |
| Theory of Operation | 2-2-1 | 36 |
| System Protocol, Basic | 2-2-1 | 2 |

| Title | Chapter/Section/Subject | Page |
|---|---|---|
| Table of S-1403C I/O Connectors | Appendix A | 1 |
| Test Equipment Requirements | Appendix C | 1 |
| Theory of Operation | 2-2-1 | 1 |
| Functional Theory of Operation | 2-2-1 | 3 |
| Module Theory of Operation | 2-2-1 | 8 |
| System Theory of Operation | 2-2-1 | 1 |
| Troubleshooting | 2-2 | |
| Video Detector PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 21 |
| Circuit Schematic | 2-2-3 | 21 |
| Disassembly | 2-3-1 | 21 |
| Theory of Operation | 2-2-1 | 44 |
| Video Filter PC Board Assembly | | |
| Assembly Drawing | 2-2-3 | 24 |
| Circuit Schematic | 2-2-3 | 25, 27 |
| Disassembly | 2-3-1 | 17 |
| Theory of Operation | 2-2-1 | 44 |
| Visual Inspection | 2-1-1 | 2 |

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